TPD1E10B06 单通道 ESD 保护二极管

1 特性

- 可为低电压 I/O 接口提供系统级 ESD 保护
- IEC 61000-4-2 4 级 ESD 保护
  - ±30kV 接触放电
  - ±30kV 气隙放电
- IEC 61000-4-5 浪涌：6A (8μs/20μs)
- I/O 电容 12pF（典型值）
- R_{DYN} 0.4Ω（典型值）
- 直流击穿电压 ±6V（最小值）
- 超低泄漏电流 100nA（最大值）
- 10V 钳位电压（I_{PP} = 1A 时的最大值）
- 工业温度范围：–40°C 至 125°C
- 小型 0402 封装尺寸
  (1mm × 0.6mm × 0.5mm)
- 业界通用 SOD-523 封装
  (0.8mm × 1.2mm)

2 应用

- 终端设备：
  - 便携式设备
  - 可穿戴设备
  - 机顶盒
  - 电子销售终端 (EPOS)
  - 电器
  - 楼宇自动化
- 接口：
  - 音频线路
  - 按钮
  - 通用输入或输出 (GPIO)

3 说明

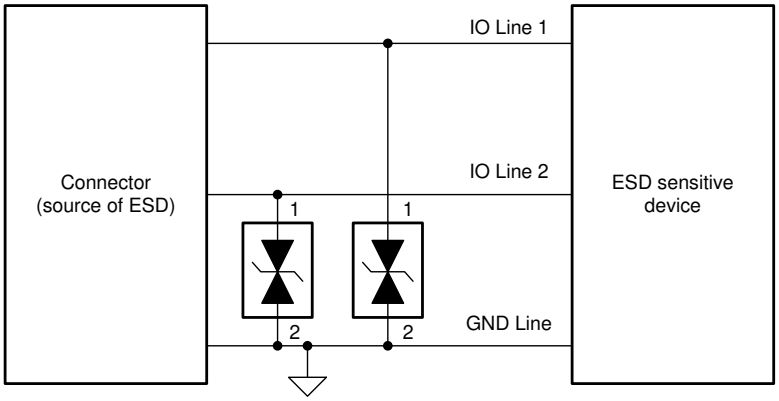
TPD1E10B06 是一款单通道 ESD TVS 二极管，提供适合空间受限应用的小型 0402 封装，以及业界通用的 SOD-523 封装。这款 TVS 保护产品提供 ±30kV 接触 ESD 和 ±30kV IEC 气隙保护，并具有一个带背靠背 TVS 二极管的 ESD 钳位电路，用于支持双极或双向信号。该 ESD 保护二极管的 12pF 线路电容适用于能够支持高达 400Mbps 数据传输速率的各种应用。

该 ESD 保护产品的典型应用是用作音频线路（麦克风、耳机和扬声器）、SD 接口、键盘或其他按钮、USB 端口的 VBUS 引脚和 ID 引脚以及通用 I/O 端口的保护电路。该 ESD 钳位电路适合用于保护便携式设备、可穿戴设备、机顶盒、电子销售终端设备、电器以及楼宇自动化产品等终端设备。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD1E10B06	X1SON (2)	0.60mm x 1.00mm
	SOD-523 (2)	0.80mm × 1.20mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



应用原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (June 2021) to Revision F (October 2021) — **Page**

- 更新了*应用原理图*.....1
- Updated the Description of Pin 1 and pin 2 in the *Pin Configuration and Functions* section.....4
- Changed HBM spec to per JS-001.....5
- Changed CDM spec to per JESD22-C101.....5
- Changed HBM spec to Q101-001.....5
- Changed CDM spec to Q101-005.....5
- Updated the *Typical Application Schematic* figure.....10
- Changed the system-level ESD protection from: *±20 kV Contact/± 25 kV Air-Gap* to: *±8 kV Contact/± 15 kV Air-Gap*.....11

Changes from Revision D (Novemeber 2015) to Revision E (June 2021) — **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 添加了 DYA 封装.....1
- 更新了*特性*部分.....1
- 更新了*应用*部分.....1
- 更新了*描述*部分.....1
- Added Thermal information for DYA package.....5
- Updated the *Overview* section.....9
- Updated the *Functional Block Diagram* section.....9
- Updated the *Feature Description* section.....9

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- Added frequency test condition to capacitance specification.....6

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- 添加了*引脚配置和功能*部分、*ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分.....1

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• Added THERMAL INFORMATION table	5

Changes from Revision * (February 2011) to Revision A (March 2012)	Page
• Added graphs to TYPICAL CHARACTERISTICS section	7
• Added APPLICATION INFORMATION section	10

5 Pin Configuration and Functions

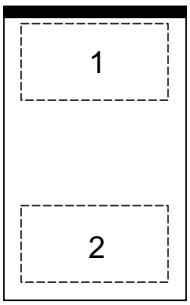


**图 5-1. DPY Package
2-Pin X1SON
Top View**

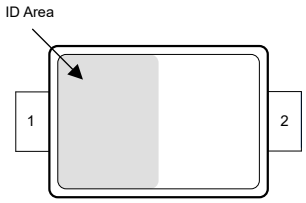


**图 5-2. DYA Package
2-Pin SOD-523
Top View**

表 5-1. Pin Functions

PIN	I/O	DESCRIPTION
1	I/O	ESD Protected I/O. Connect other pin ground.
2		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		90	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		6	A
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge - DPY	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101	±1000	V
$V_{(ESD)}$	Electrostatic discharge - DYA	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002	±1000	V

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating voltage	Pin 1 to 2 or Pin 2 to 1	–5.5		5.5	V
T_A	Operating free-air temperature	-40		125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD1E10B06		UNIT
		DPY (X1SON)	DYA (SOD523)	
		2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	615.5	730.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	404.8	413.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	493.3	497.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	127.7	129.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	493.3	491.8	°C/W

6.5 Thermal Information (continued)

THERMAL METRIC[1]		TPD1E10B06		UNIT
		DPY (X1SON)	DYA (SOD523)	
		2 PINS	2 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	162	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	Pin 1 to 2 or Pin 2 to 1			5.5	V
I_{LEAK}	Leakage current	Pin 1 = 5 V, Pin 2 = 0 V			100	nA
$V_{Clamp1,2}$	Clamp voltage with surge strike on pin 1, pin 2 grounded.	I_{PP} = 1 A, t_p = 8/20 µs[2]			10	V
$V_{Clamp1,2}$	Clamp voltage with surge strike on pin 1, pin 2 grounded.	I_{PP} =5 A, t_p = 8/20 µs[2]			14	V
$V_{Clamp2,1}$	Clamp voltage with surge strike on pin 2, pin 1 grounded.	I_{PP} = 1 A, t_p = 8/20 µs[2]			8.5	V
		I_{PP} = 5 A, t_p = 8/20 µs[2]			14	
R_{DYN}	Dynamic resistance	Pin 1 to Pin 2[1]		0.32		Ω
		Pin 2 to Pin 1[1]		0.38		
C_{IO}	I/O capacitance	V_{IO} = 2.5 V; f = 1 MHz		12		pF
$V_{BR1,2}$	Break-down voltage, pin 1 to pin 2	I_{IO} = 1 mA	6			V
$V_{BR2,1}$	Break-down voltage, pin 2 to pin 1	I_{IO} = 1 mA	6			V

(1) Extraction of R_{DYN} using least squares fit of TLP characteristics between I_{PP} = 10 A and I_{PP} = 20 A.
(2) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5

6.7 Typical Characteristics

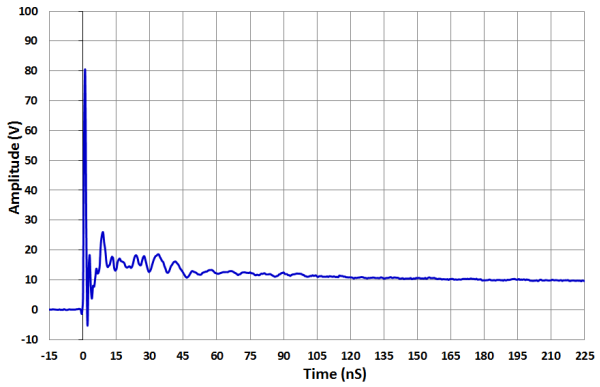


图 6-1. IEC 61000-4-2 Clamp Voltage +8 kV Contact ESD

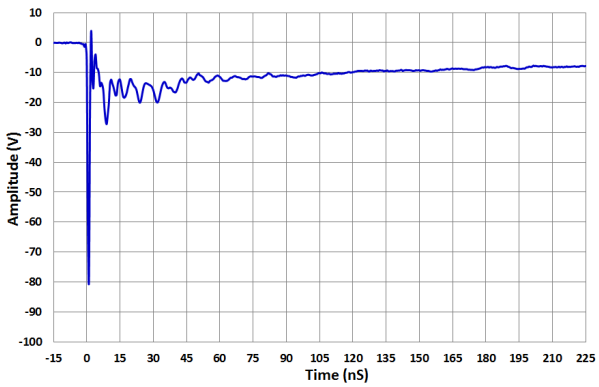


图 6-2. IEC 61000-4-2 Clamp Voltage –8-kV Contact ESD

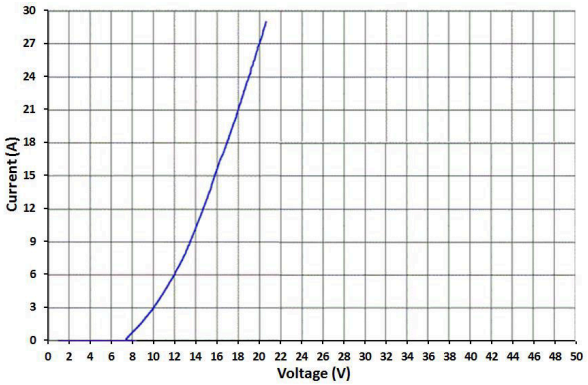


图 6-3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2

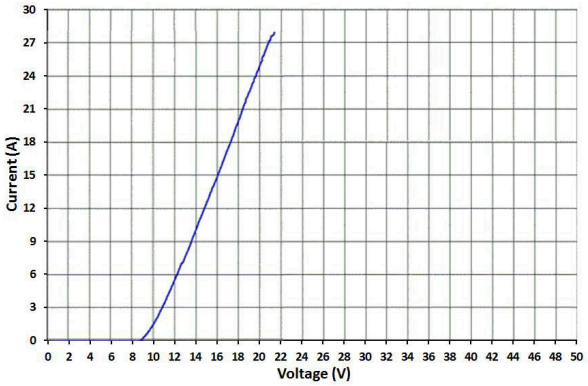


图 6-4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1

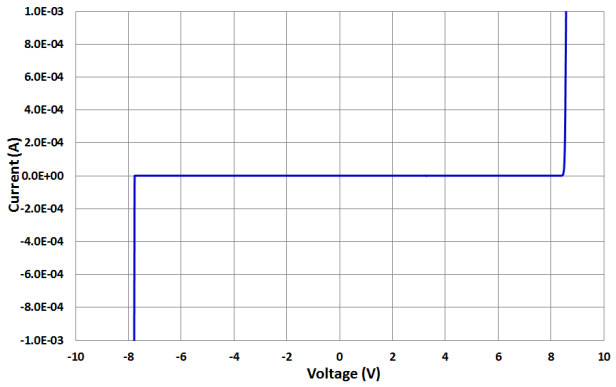


图 6-5. IV Curve

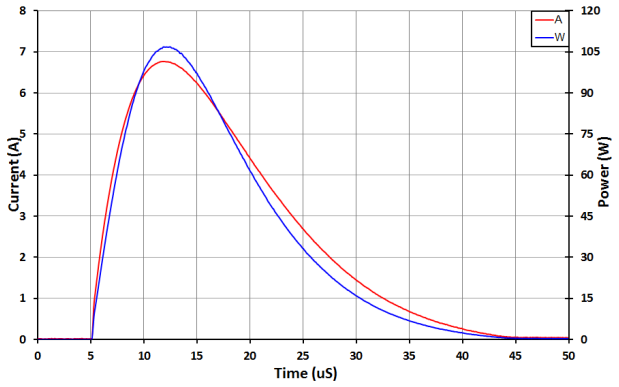


图 6-6. Positive Surge Waveform 8 to 20 µs

6.7 Typical Characteristics (continued)

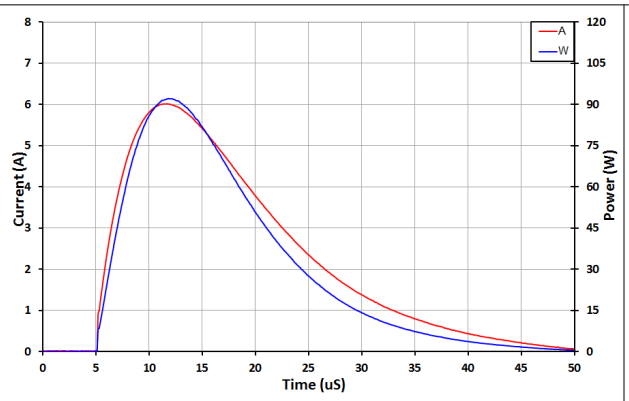


图 6-7. Negative Surge Waveform 8 to 20 µs

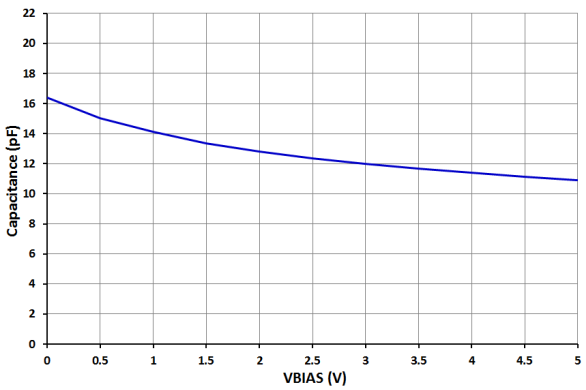


图 6-8. Pin Capacitance Across V_{BIAS}

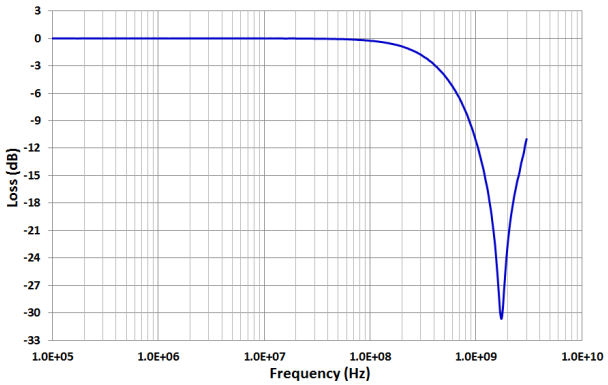


图 6-9. Insertion Loss

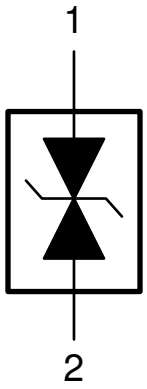
7 Detailed Description

7.1 Overview

The TPD1E108B06 is a single-channel ESD TVS diode in a small 0402 package convenient for space constrained applications and an industry standard SOD-523 package. This TVS protection product offers ±30 kV IEC air-gap, ±30 kV contact ESD protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12 pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps.

Typical application of this ESD protection product is the circuit protection for audio lines (microphone, earphone, and speakerphone), SD interfacing, keypad or other buttons, VBUS pin and ID pin of USB ports, and general-purpose I/O ports. This ESD clamp is a good fit for the protection of the end equipment like ebooks, tablets, remote controllers, wearables, set-top boxes, and electronic point of sale equipment.

7.2 Functional Block Diagram



7.3 Feature Description

TPD1E10B06 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to ±30 kV contact and ±30 kV air-gap specified in the IEC 61000-4-2 international standard. The device can also handle up to 6-A surge current (IEC61000-4-5 8/20 µs). The I/O capacitance of 12 pF supports a data rate up to 400 Mbps. This clamping device has a small dynamic resistance of 0.4 Ω typically, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 10 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO and especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the V_{RWM}. The industrial temperature range of –40°C to 125°C makes this ESD device work at extensive temperatures in most environments. The 0402 package can fit into small electronic devices like mobile equipment and wearables whereas the SOD-523 package is good for industrial applications.

7.4 Device Functional Modes

TPD1E10B06 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below V_{RWM} and activates when the voltage between pin 1 and pin 2 goes above V_{BR}. During IEC ESD events, transient voltages as high as ±30 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

When a system contains a human interface connector, the system becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. TPD1E10B06 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

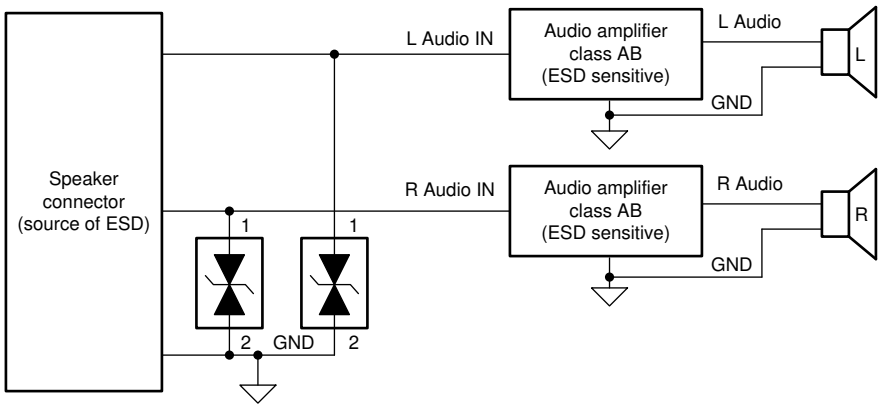


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, two TPD1E10B06s will be used to protect left and right audio channels. For this audio application, the following system parameters are known.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Audio Amplifier Class	AB
Audio signal voltage range	– 3 V to 3 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD Protection	±20 kV Contact/ ±25 kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- Voltage range on the protected line must not exceed the reverse standoff voltage of one or more TVS diodes (V_{RWM})
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode

For this application, the audio signal voltage range is –3 V to 3 V. The V_{RWM} for the TVS is –5.5 V to 5.5 V; therefore, the bidirectional TVS will not break down during normal operation, and therefore normal operation of the audio signal will not be effected due to the signal voltage range. In this application, a bidirectional TVS like TPD1E10B06 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; ensure that the TVS I/O capacitance will not distort this signal by filtering it. With TPD1E10B06 typical capacitance of 12 pF, which leads to a typical 3-dB bandwidth of 400 MHz, this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires above standard Level 4 IEC 61000-4-2 system-level ESD protection (±8 kV Contact/ ±15 kV Air-Gap). A standard TVS cannot survive this level of IEC ESD stress. However, TPD1E10B06 can survive at least ±30 kV Contact/ ±30 kV Air-Gap. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide the full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, a system designer must use proper board layout of their TVS ESD protection diodes. See *节 10* for instructions on properly laying out TPD1E10B06.

8.2.3 Application Curves

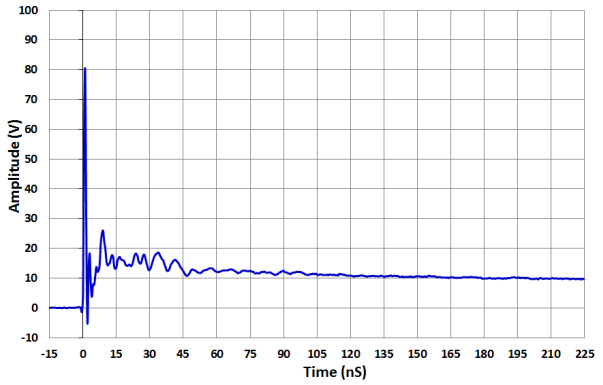


图 8-2. IEC 61000-4-2 Clamp Voltage +8 kV Contact ESD

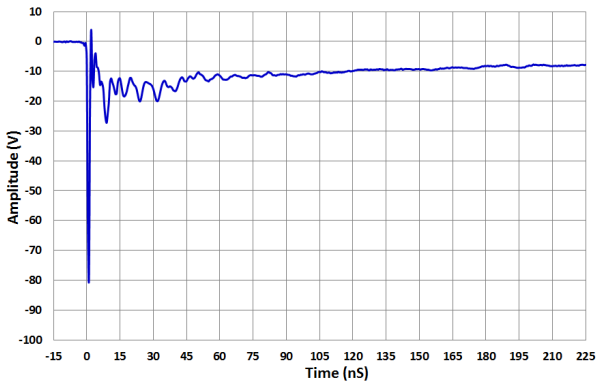


图 8-3. IEC 61000-4-2 Clamp Voltage –8 kV Contact ESD

9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, therefore there is no requirement to power it. Take care to make sure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path

10.2 Layout Example

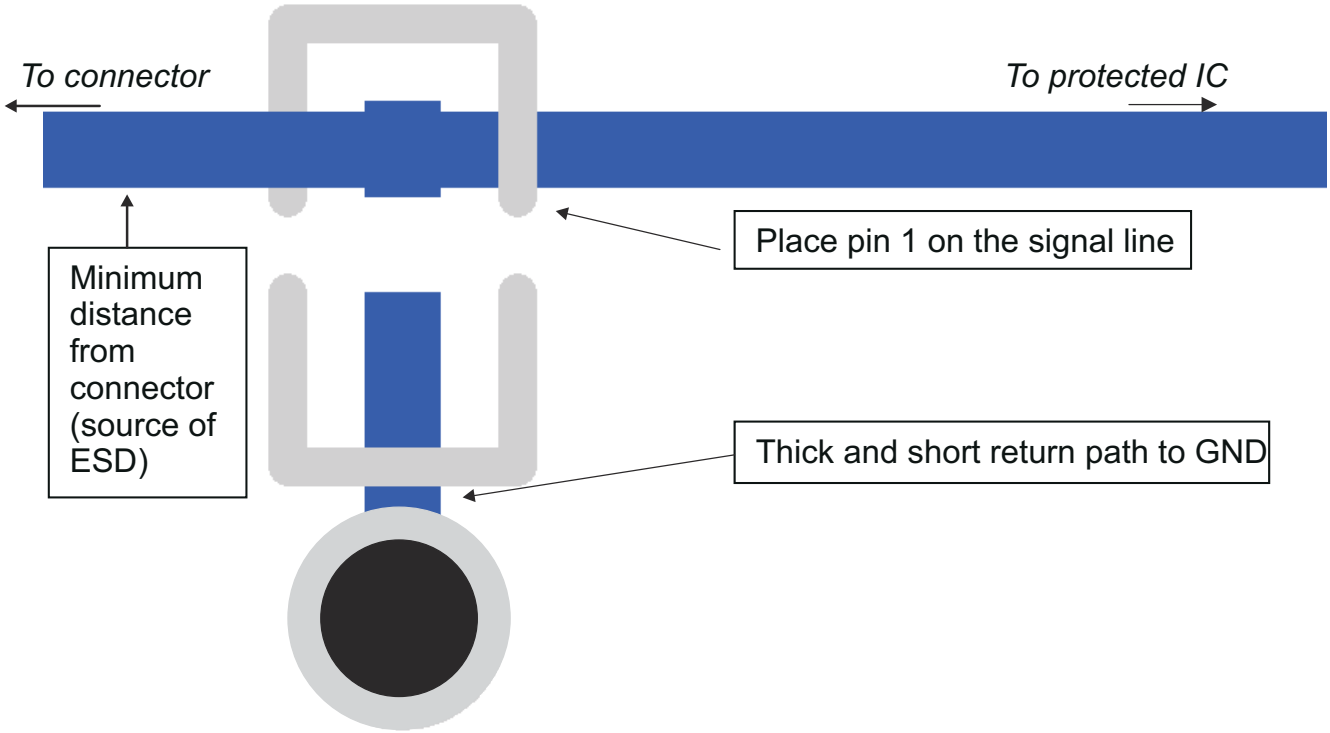


图 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E10B06DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B1, B2, B6, BI)	Samples
TPD1E10B06DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B1, B2, B6, BI)	Samples
TPD1E10B06DYAR	ACTIVE	SOT-5X3	DYA	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	1KF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD1E10B06 :

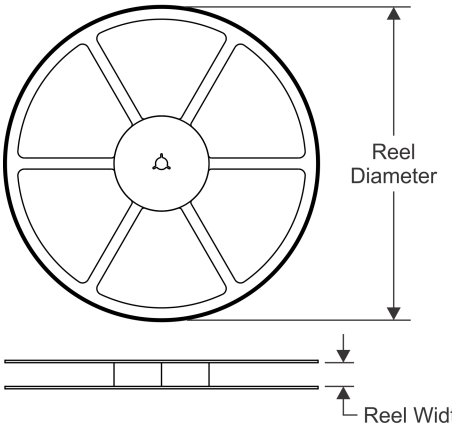
- Automotive : TPD1E10B06-Q1

NOTE: Qualified Version Definitions:

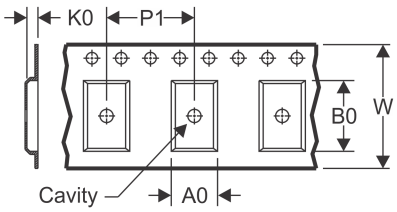
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

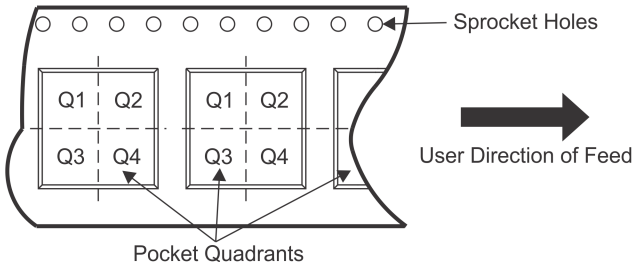


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

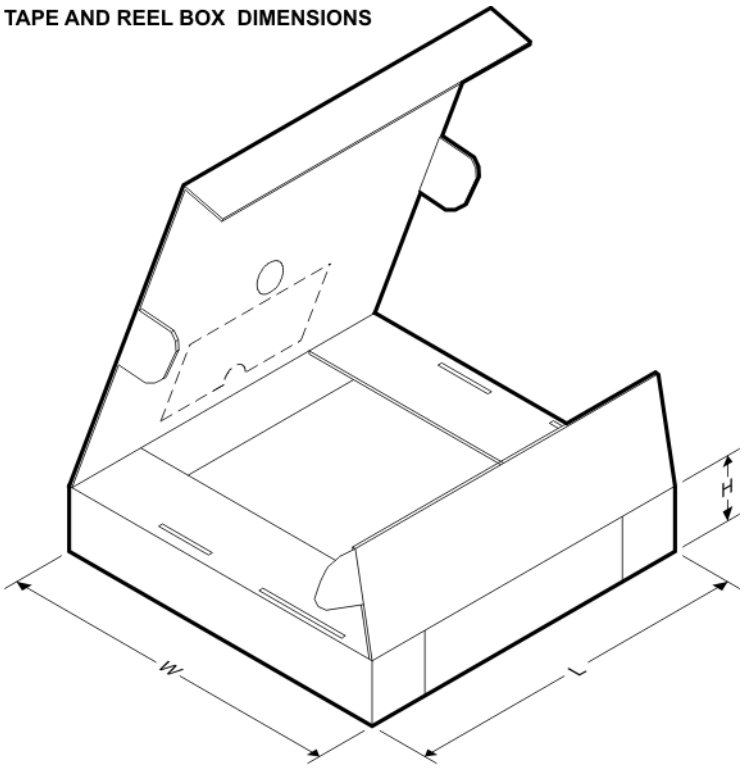
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E10B06DPYR	X1SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B06DPYR	X1SON	DPY	2	10000	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E10B06DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TPD1E10B06DPYR	X1SON	DPY	2	10000	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1
TPD1E10B06DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B06DPYT	X1SON	DPY	2	250	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E10B06DPYT	X1SON	DPY	2	250	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1
TPD1E10B06DPYT	X1SON	DPY	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TPD1E10B06DYAR	SOT-5X3	DYA	2	3000	178.0	9.5	0.5	1.94	0.73	4.0	8.0	Q1

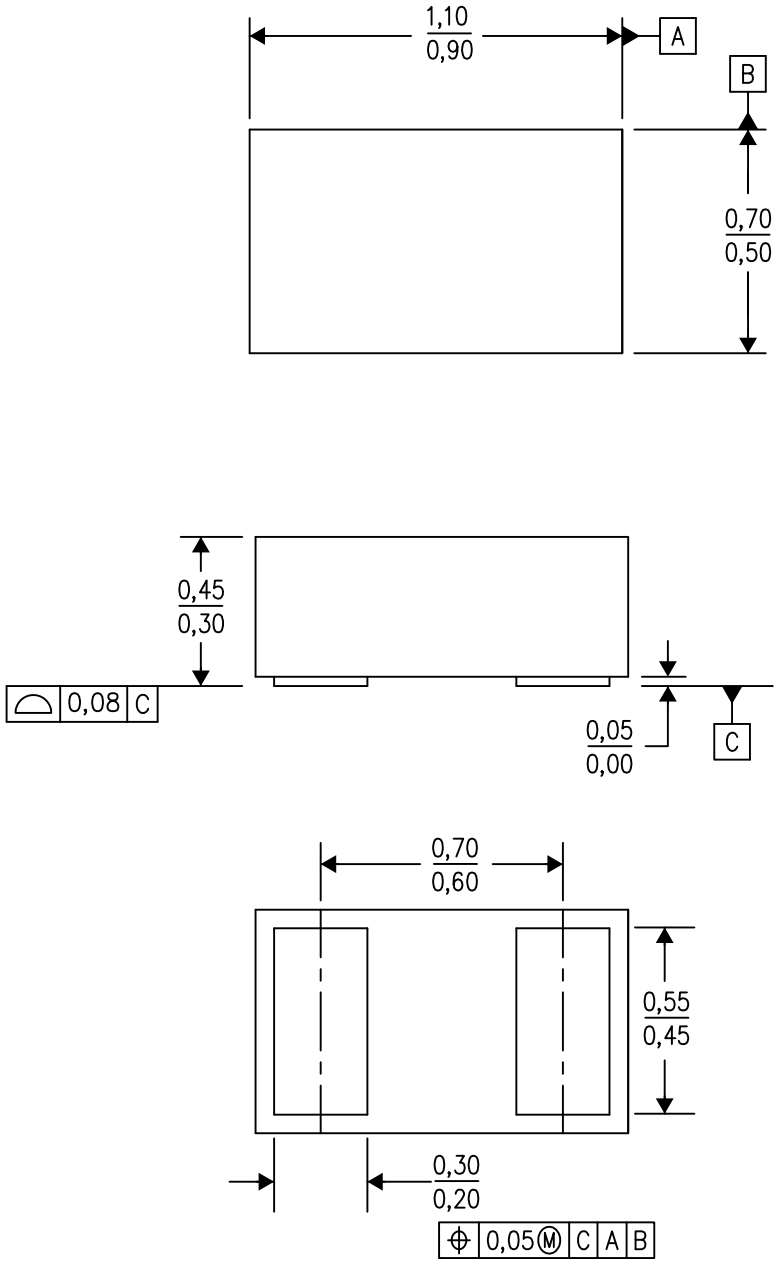
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E10B06DPYR	X1SON	DPY	2	10000	184.0	184.0	19.0
TPD1E10B06DPYR	X1SON	DPY	2	10000	203.2	196.8	33.3
TPD1E10B06DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0
TPD1E10B06DPYR	X1SON	DPY	2	10000	189.0	185.0	36.0
TPD1E10B06DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E10B06DPYT	X1SON	DPY	2	250	203.2	196.8	33.3
TPD1E10B06DPYT	X1SON	DPY	2	250	189.0	185.0	36.0
TPD1E10B06DPYT	X1SON	DPY	2	250	205.0	200.0	33.0
TPD1E10B06DYAR	SOT-5X3	DYA	2	3000	210.0	200.0	42.0

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



4211012/D 08/14

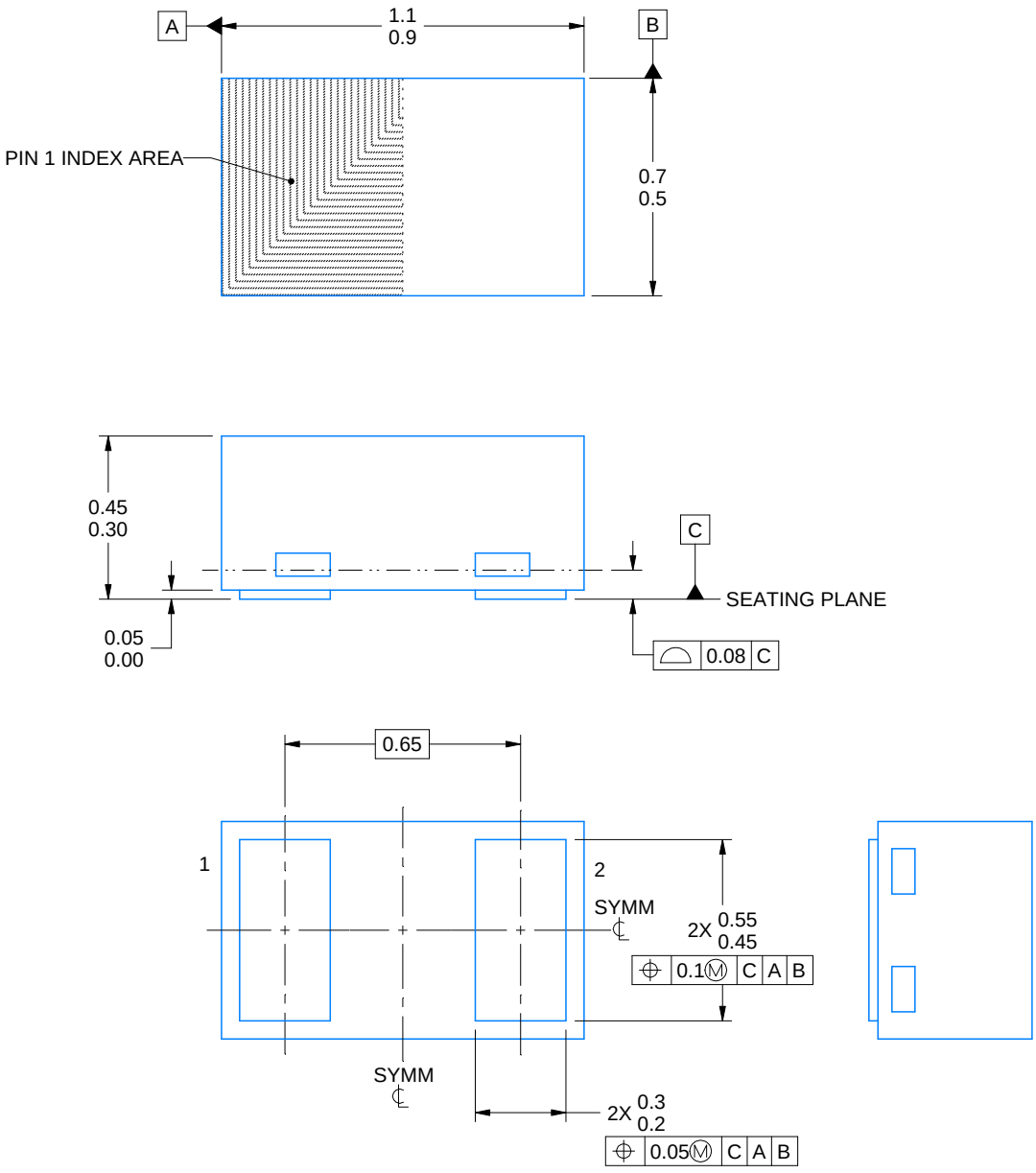
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

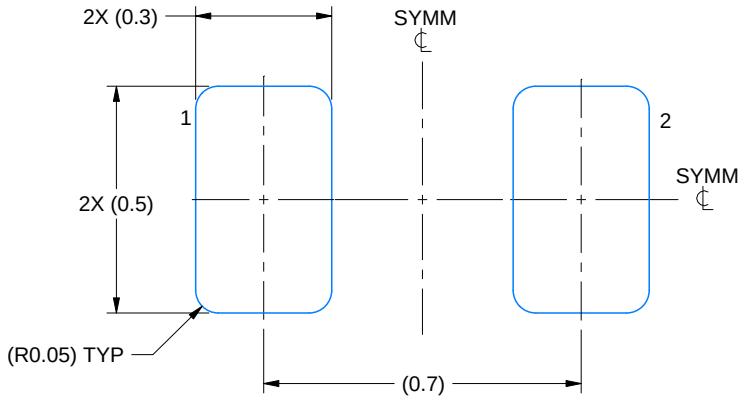
PLASTIC SMALL OUTLINE - NO LEAD



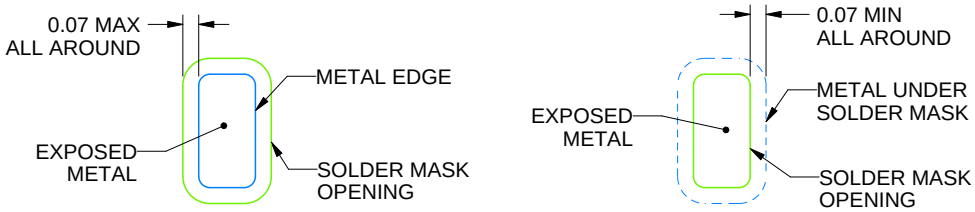
4224561/B 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

4224561/B 03/2021

NOTES: (continued)

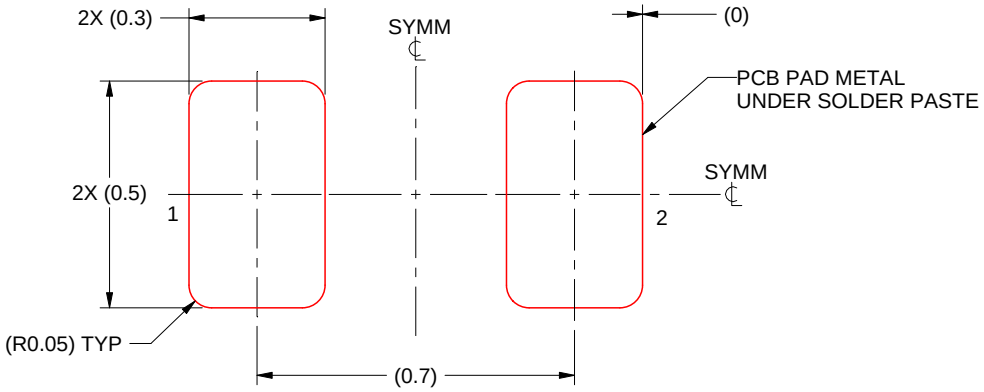
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/B 03/2021

NOTES: (continued)

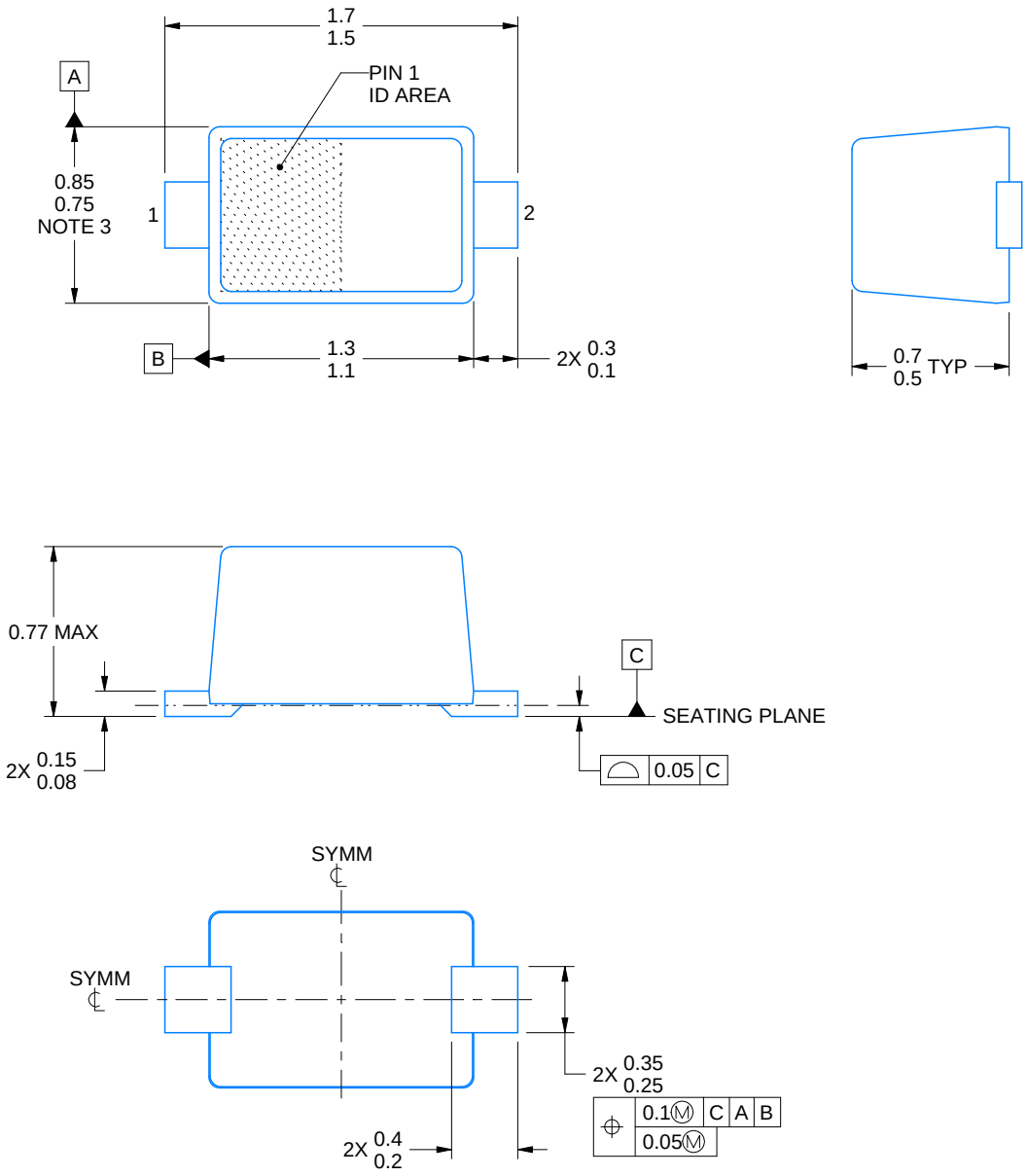
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

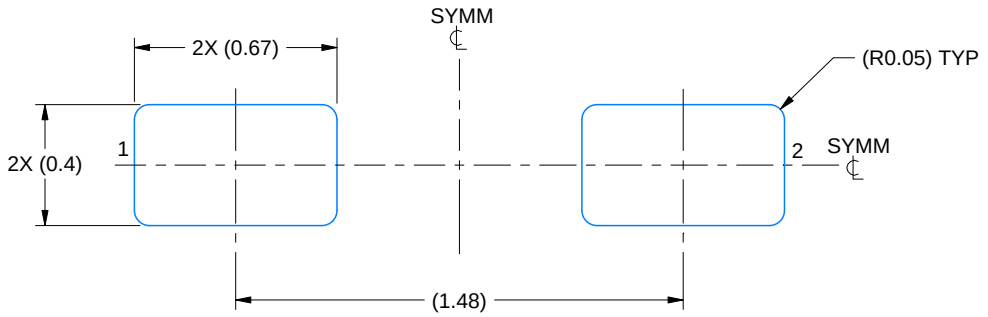
PLASTIC SMALL OUTLINE



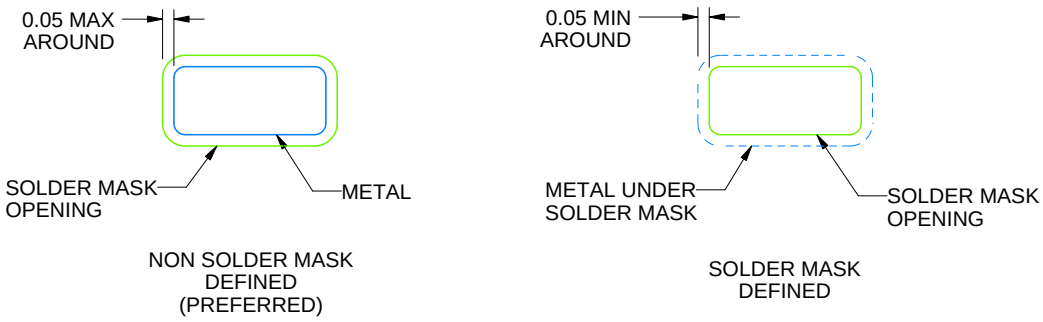
4224978/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

4224978/B 09/2021

NOTES: (continued)

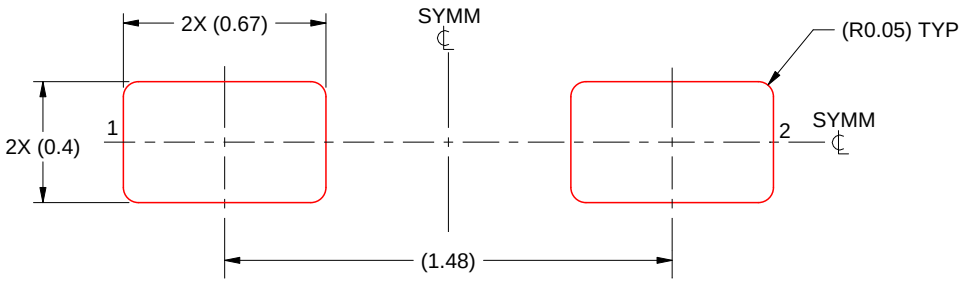
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/B 09/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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