

SNx4ACT244 Octal Buffers and Drivers With 3-State Outputs

1 Features

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 9.5 ns at 5 V
- Inputs are TTL Compatible
- On Products Compliant to MIL-PRF-38535, All Parameters are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- LED displays
- Servers and Telecommunication
- Switching Networks

3 Description

These SNx4ACT244 octal buffers and drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

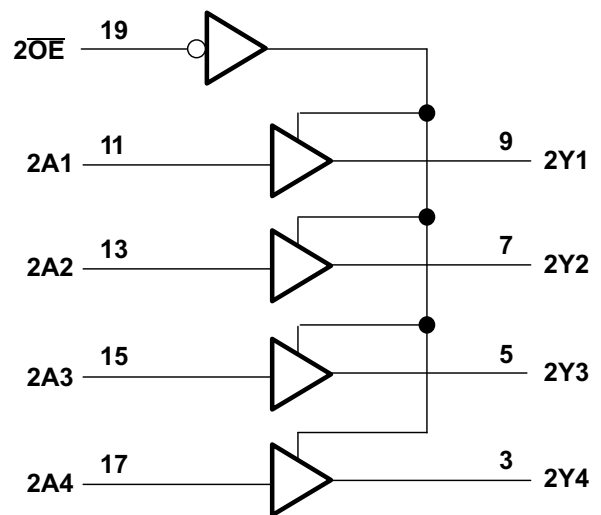
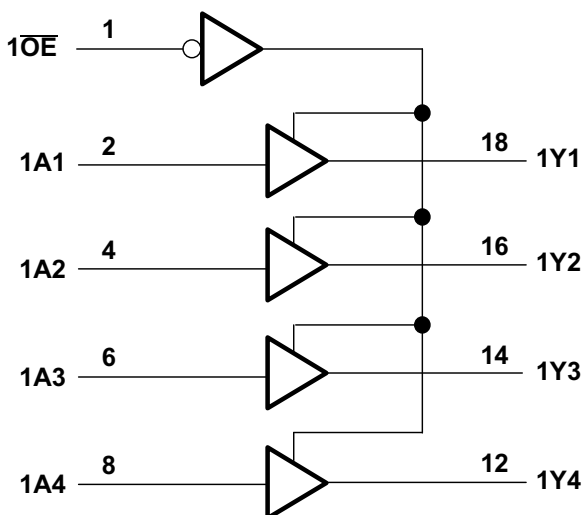
The SNx4ACT244 devices are organized as two 4-bit buffers and drivers with separate output-enable (OE) inputs. When OE is low, the device passes non-inverted data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------|------------|--------------------|
| SN74ACT244DB | SSOP (20) | 7.20 mm × 5.30 mm |
| SN74ACT244DW | SOIC (20) | 12.80 mm × 7.50 mm |
| SN74ACT244N | PDIP (20) | 24.33 mm × 6.35 mm |
| SN74ACT244NS | SO (20) | 12.60 mm × 7.80 mm |
| SN74ACT244PW | TSSOP (20) | 6.50 mm × 6.40 mm |
| SNJ54ACT244FK | LCCC (20) | 8.89 mm × 8.89 mm |
| SNJ54ACT244J | CDIP (20) | 24.20 mm × 6.92 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

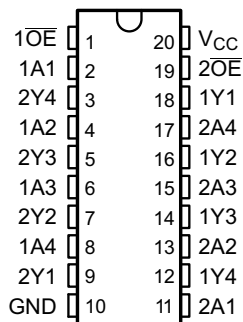
Changes from Revision C (October 2002) to Revision D

Page

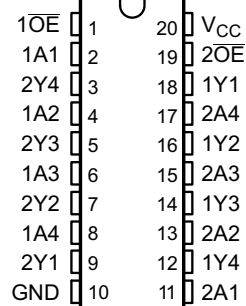
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**

5 Pin Configuration and Functions

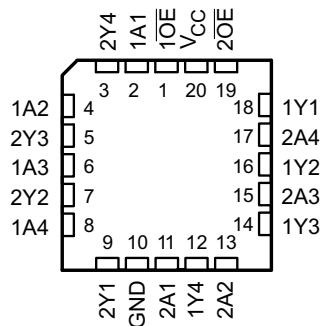
SN54ACT244: J or W Packages
20-Pin CDIP or CFP
Top View



SN74ACT244: DB, DW, N, NS, or PW Packages
20-Pin SSOP, SOIC, PDIP, SO, or TSSOP
Top View



SN54ACT244: FK Package
20-Pin LCCC
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|------|-----|----------------------------|
| NO. | NAME | | |
| 1 | 1OE | I | 1 Active low Output enable |
| 2 | 1A1 | I | 1A1 input |
| 3 | 2Y4 | O | 2Y4 output |
| 4 | 1A2 | I | 1A2 input |
| 5 | 2Y3 | O | 2Y3 Output |
| 6 | 1A3 | I | 1A3 input |
| 7 | 2Y2 | O | 2Y2 Output |
| 8 | 1A4 | I | 1A4 input |
| 9 | 2Y1 | O | 2Y1 Output |
| 10 | GND | — | Ground |
| 11 | 2A1 | I | 2A1 input |
| 12 | 1Y4 | O | 1Y4 output |
| 13 | 2A2 | I | 2A2 input |
| 14 | 1Y3 | O | 1Y3 Output |
| 15 | 2A3 | I | 2A3 input |
| 16 | 1Y2 | O | 1Y2 Output |
| 17 | 2A4 | I | 2A4 input |
| 18 | 1Y1 | O | 1Y1 Output |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-----|------------------|-----|----------------------------|
| NO. | NAME | | |
| 19 | $\overline{2OE}$ | I | 2 Active low Output enable |
| 20 | V_{CC} | — | Power |

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------|--|-----------------------------|----------------|------------|
| V_{CC} | Supply voltage | −0.5 | 7 | V |
| V_I | Input voltage ⁽²⁾ | −0.5 | $V_{CC} + 0.5$ | V |
| V_O | Output voltage ⁽²⁾ | −0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 mA |
| I_{OK} | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | | ±50 mA |
| | Continuous current through V_{CC} or GND | | | ±200 mA |
| T_J | Absolute Maximum Junction Temperature | | | 150 °C |
| T_{stg} | Storage temperature | −65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

| | | VALUE | UNIT |
|---|-------------------------|--|------------|
| SN74ACT244 in DW Package | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±3000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±2000 |
| SN54ACT244 in J, W, DB, N, NS, PW, FK Packages | | | |
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|------------|----------|------|
| V_{CC} | Supply voltage | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | −24 | mA |
| I_{OL} | Low-level output current | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 8 | ns/V |
| T_A | Operating free-air temperature | SN54ACT244 | −55 | 125 |
| | | SN74ACT244 | −40 | 85 |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74ACT244 | | | | | UNIT | |
|-------------------------------|--|-----------|----------|---------|------------|------|------|
| | DB (SSOP) | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | | |
| | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 94.1 | 81.4 | 48.1 | 76.4 | 103 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 55.6 | 46.8 | 34.1 | 42.6 | 37.7 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 49.3 | 49.3 | 29 | 43.9 | 54 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 20.8 | 20 | 19.5 | 18.8 | 2.8 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 48.9 | 48.8 | 28.9 | 43.5 | 53.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|-----------------------|-------|------|-------|-------|
| V _{OH} | I _{OH} = -50 μA | T _A = 25°C | 4.5 V | 4.4 | 4.49 | V |
| | | SN54ACT244 | | 4.4 | | |
| | | SN74ACT244 | | 4.4 | | |
| | | T _A = 25°C | 5.5 V | 5.4 | 5.49 | |
| | | SN54ACT244 | | 5.4 | | |
| | | SN74ACT244 | | 5.4 | | |
| | I _{OH} = -24 mA | T _A = 25°C | 4.5 V | 3.86 | | |
| | | SN54ACT244 | | 3.7 | | |
| | | SN74ACT244 | | 3.76 | | |
| | | T _A = 25°C | 5.5 V | 4.86 | | |
| | | SN54ACT244 | | 4.7 | | |
| | | SN74ACT244 | | 4.76 | | |
| I _{OH} = -50 mA ⁽¹⁾ | SN54ACT244 | 5.5 V | 3.85 | | | |
| I _{OH} = -75 mA ⁽¹⁾ | SN74ACT244 | 5.5 V | 3.85 | | | |
| V _{OL} | I _{OL} = 50 μA | T _A = 25°C | 4.5 V | | 0.001 | 0.1 |
| | | SN54ACT244 | | | 0.1 | |
| | | SN74ACT244 | | | 0.1 | |
| | | T _A = 25°C | 5.5 V | | 0.001 | 0.1 |
| | | SN54ACT244 | | | 0.1 | |
| | | SN74ACT244 | | | 0.1 | |
| | I _{OL} = 24 mA | T _A = 25°C | 4.5 V | | | 0.36 |
| | | SN54ACT244 | | | 0.5 | |
| | | SN74ACT244 | | | 0.44 | |
| | | T _A = 25°C | 5.5 V | | | 0.36 |
| | | SN54ACT244 | | | 0.5 | |
| | | SN74ACT244 | | | 0.44 | |
| I _{OL} = 50 mA ⁽¹⁾ | SN54ACT244 | 5.5 V | | | 1.65 | |
| I _{OL} = 75 mA ⁽¹⁾ | SN74ACT244 | 5.5 V | | | 1.65 | |
| I _{OZ} | V _O = V _{CC} or GND | T _A = 25°C | 5.5 V | | | ±0.25 |
| | | SN54ACT244 | | | | ±5 |
| | | SN74ACT244 | | | | ±2.5 |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------------|---|-----------------------|-----------------|-----|-----|------|------|
| I _I | V _I = V _{CC} or GND | T _A = 25°C | 5.5 V | | | ±0.1 | μA |
| | | SN54ACT244 | | | | ±1 | |
| | | SN74ACT244 | | | | ±1 | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | T _A = 25°C | 5.5 V | | | 4 | μA |
| | | SN54ACT244 | | | | 80 | |
| | | SN74ACT244 | | | | 40 | |
| ΔI _{CC} ⁽²⁾ | One input at 3.4 V, Other inputs at GND or V _{CC} | T _A = 25°C | 5.5 V | | 0.6 | | mA |
| | | SN54ACT244 | | | | 1.6 | |
| | | SN74ACT244 | | | | 1.5 | |
| C _I | V _I = V _{CC} or GND | T _A = 25°C | 5 V | | 2.5 | | pF |
| C _O | V _I = V _{CC} or GND | T _A = 25°C | 5 V | | 8 | | pF |

 (2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.6 Switching Characteristics

 over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--------------|-------------|-----------------------|-----|------|------|------|
| t _{PLH} | A | Y | T _A = 25°C | 2 | 6.5 | 9 | ns |
| | | | SN54ACT244 | 1 | | 10 | |
| | | | SN74ACT244 | 1.5 | | 10 | |
| T _A = 25°C | | | 2 | 7 | 9 | | |
| SN54ACT244 | | | 1 | | 10 | | |
| SN74ACT244 | | | 1.5 | | 10 | | |
| t _{PHL} | A | Y | T _A = 25°C | 2 | 7 | 9 | ns |
| | | | SN54ACT244 | 1 | | 10 | |
| | | | SN74ACT244 | 1.5 | | 10 | |
| T _A = 25°C | | | 1.5 | 7 | 8.5 | | |
| SN54ACT244 | | | 1 | | 9.5 | | |
| SN74ACT244 | | | 1 | | 9.5 | | |
| t _{PZH} | OE | Y | T _A = 25°C | 1.5 | 7 | 8.5 | ns |
| | | | SN54ACT244 | 1 | | 9.5 | |
| | | | SN74ACT244 | 1 | | 9.5 | |
| T _A = 25°C | | | 2 | 7 | 9.5 | | |
| SN54ACT244 | | | 1 | | 11 | | |
| SN74ACT244 | | | 1.5 | | 10.5 | | |
| t _{PZL} | OE | Y | T _A = 25°C | 2 | 8 | 9.5 | ns |
| | | | SN54ACT244 | 1 | | 11 | |
| | | | SN74ACT244 | 1.5 | | 10.5 | |
| T _A = 25°C | | | 2.5 | 7.5 | 10 | | |
| SN54ACT244 | | | 1 | | 11.5 | | |
| SN74ACT244 | | | 2 | | 10.5 | | |

6.7 Operating Characteristics

 V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------------|--|-----|------|
| C _{pd} | Power dissipation capacitance per buffer/driver C _L = 50 pF, f = 1 MHz | 45 | pF |

6.8 Typical Characteristics

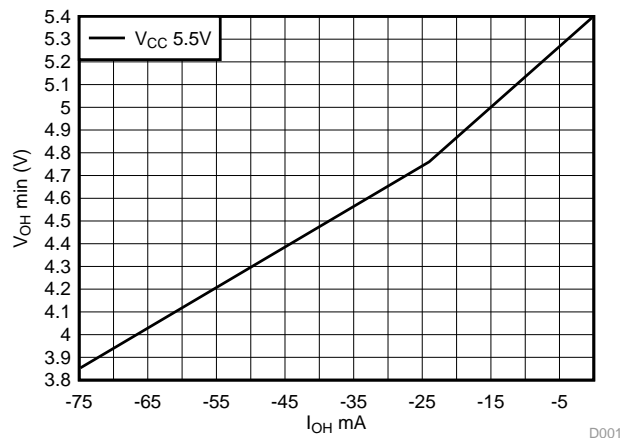
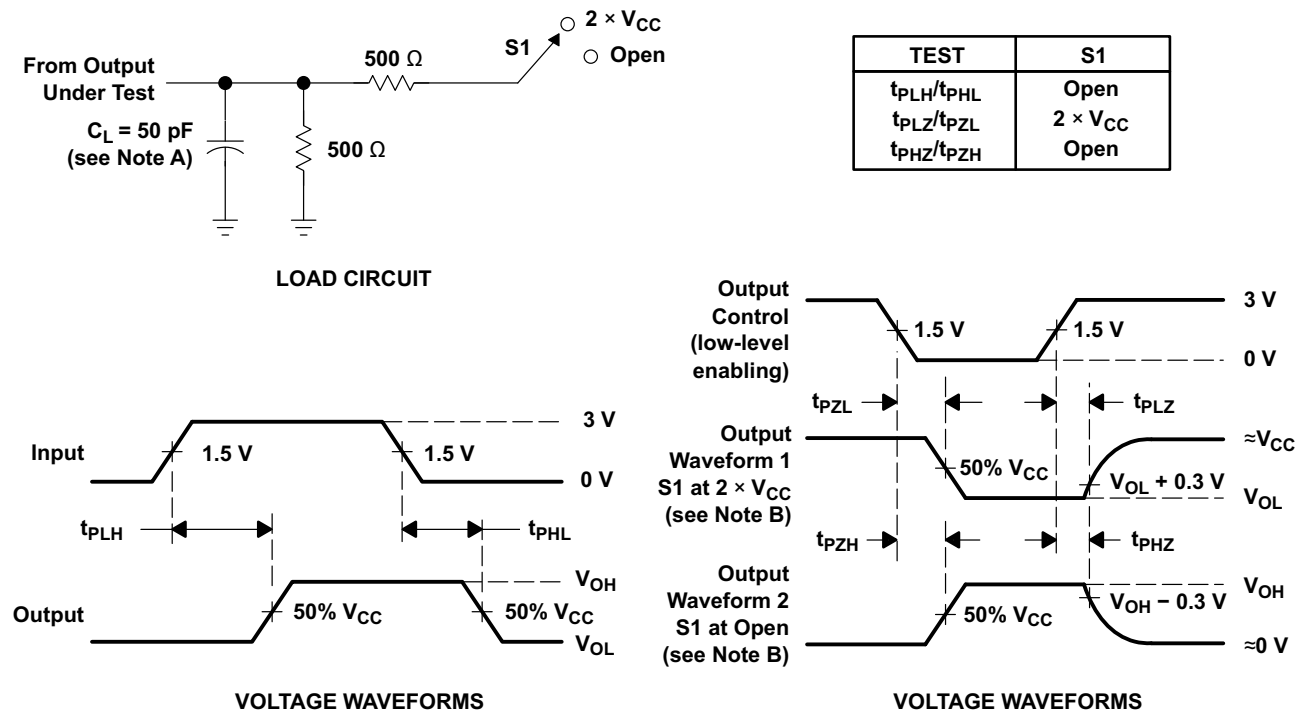


Figure 1. V_{OH} Vs I_{OH}

7 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

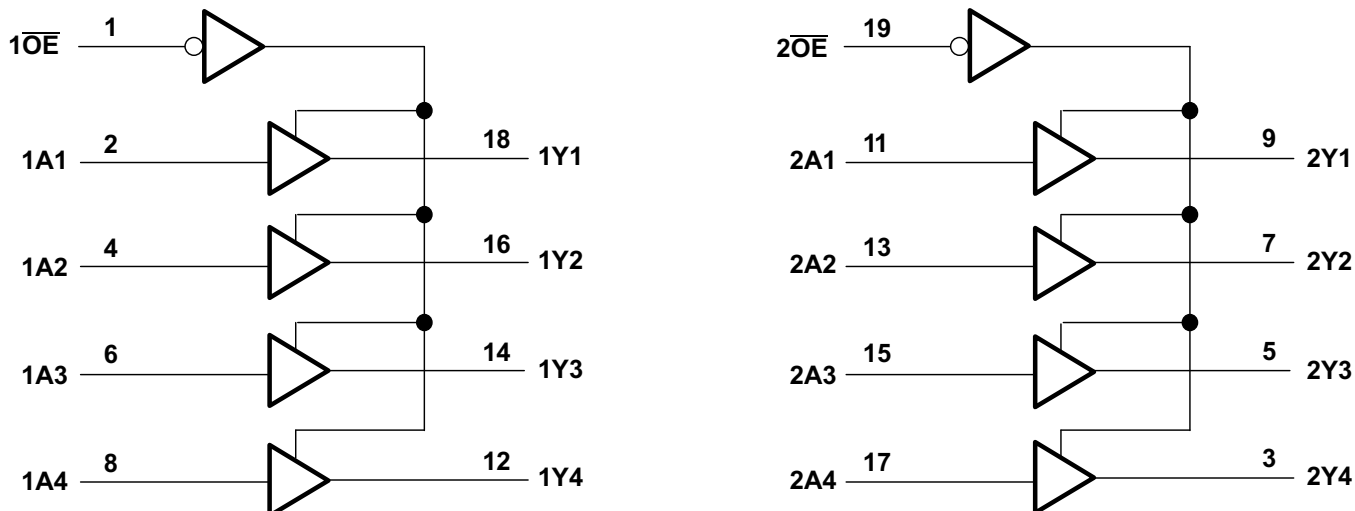
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4ACT244 devices are buffer drivers with separate output enable inputs. The active low output enable ensure the outputs are in high impedance when high. To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



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Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The SNx4ACT244 devices are recommended for 4.5 V to 5.5-V V_{CC} range under normal operating conditions. The inputs are TTL compatible accepting 2-V minimum high at 5-V V_{CC} .

8.4 Device Functional Modes

Table 1 lists the functions of the device.

Table 1. Function Table (Each Buffer)

| INPUTS | | OUTPUT Y |
|-----------------|---|-------------|
| \overline{OE} | A | |
| L | H | H |
| L | L | L |
| H | X | Hi-Z |

9 Application and Implementation

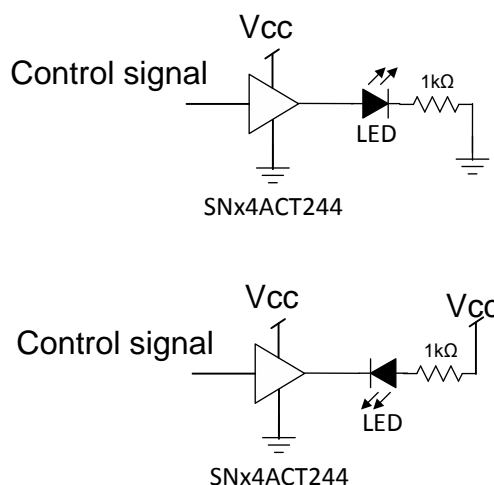
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SNx4ACT244 is high-drive buffer drivers providing 24-mA current drive per channel at nominal operating specifications. It can be used as LED driver with appropriate current-limiting resistors to ground or V_{CC} within the device's and LED's operating characteristics.

9.2 Typical Application



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Figure 4. Typical LED driving application

9.2.1 Design Requirements

The pullup and pulldown current limiting resistors are chosen to operate within the LED and the SNx4ACT244 device operating specifications. A 1-kΩ resistor, limits the current to less than 5 mA at 5-V V_{CC} operation.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For the specified high and low levels See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#).
 - Inputs are not overvoltage tolerant and must be limited to V_{CC} .
2. Recommended output conditions:
 - Limit the output voltage to V_{CC} .
 - Choose the current-limiting resistor for the LED to limit the output current to I_O as per the [Recommended Operating Conditions](#).

Typical Application (continued)

9.2.3 Application Curve

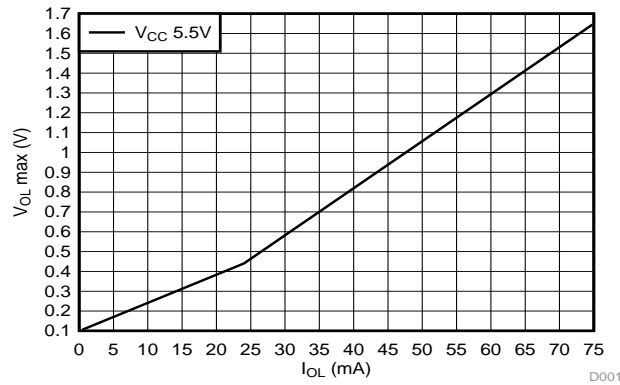


Figure 5. V_{OL} vs I_{OL}

10 Power Supply Recommendations

The power supply may be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01- μF or 0.022- μF capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

Inputs should not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in the [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

11.2 Layout Example

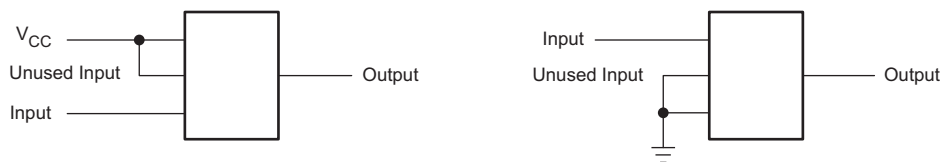


Figure 6. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54ACT244 | Click here | Click here | Click here | Click here | Click here |
| SN74ACT244 | Click here | Click here | Click here | Click here | Click here |

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------------|-------------------------|
| 5962-8776001M2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776001M2A SNJ54ACT 244FK | Samples |
| 5962-8776001MRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776001MR A SNJ54ACT244J | Samples |
| 5962-8776001MSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776001MS A SNJ54ACT244W | Samples |
| 5962-8776001SRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776001SR A SNV54ACT244J | Samples |
| 5962-8776001SSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776001SS A SNV54ACT244W | Samples |
| SN74ACT244DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD244 | Samples |
| SN74ACT244DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT244 | Samples |
| SN74ACT244DWE4 | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT244 | Samples |
| SN74ACT244DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT244 | Samples |
| SN74ACT244DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT244 | Samples |
| SN74ACT244DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT244 | Samples |
| SN74ACT244N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ACT244N | Samples |
| SN74ACT244NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74ACT244N | Samples |
| SN74ACT244NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT244 | Samples |
| SN74ACT244NSRG4 | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT244 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|--|-------------------------|
| SN74ACT244PW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD244 | Samples |
| SN74ACT244PWE4 | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD244 | Samples |
| SN74ACT244PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD244 | Samples |
| SN74ACT244PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | AD244 | Samples |
| SN74ACT244PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD244 | Samples |
| SN74ACT244PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD244 | Samples |
| SNJ54ACT244FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962- 8776001M2A SNJ54ACT 244FK | Samples |
| SNJ54ACT244J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776001MR A SNJ54ACT244J | Samples |
| SNJ54ACT244W | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8776001MS A SNJ54ACT244W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ACT244, SN54ACT244-SP, SN74ACT244 :

- Catalog : [SN74ACT244](#), [SN54ACT244](#)
- Automotive : [SN74ACT244-Q1](#), [SN74ACT244-Q1](#)
- Enhanced Product : [SN74ACT244-EP](#), [SN74ACT244-EP](#)
- Military : [SN54ACT244](#)
- Space : [SN54ACT244-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ACT244DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ACT244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74ACT244NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74ACT244PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74ACT244PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74ACT244PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ACT244DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74ACT244DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ACT244NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ACT244PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74ACT244PWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74ACT244PWRG4 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-8776001M2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 5962-8776001MSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| 5962-8776001SSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74ACT244DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74ACT244DWE4 | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74ACT244N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74ACT244NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74ACT244PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74ACT244PWE4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74ACT244PWG4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54ACT244FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ACT244W | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

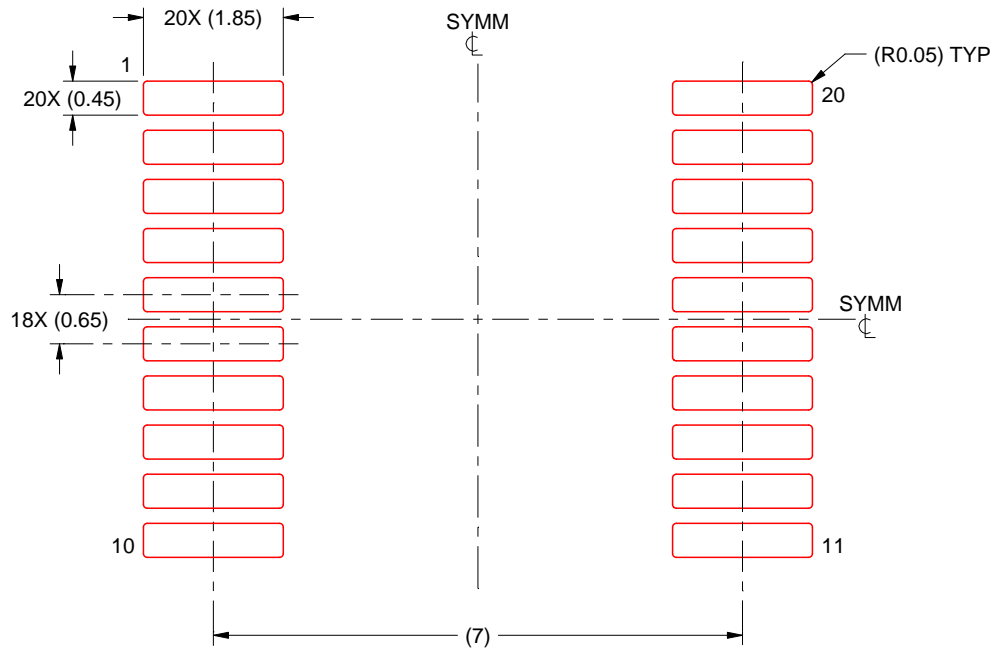
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

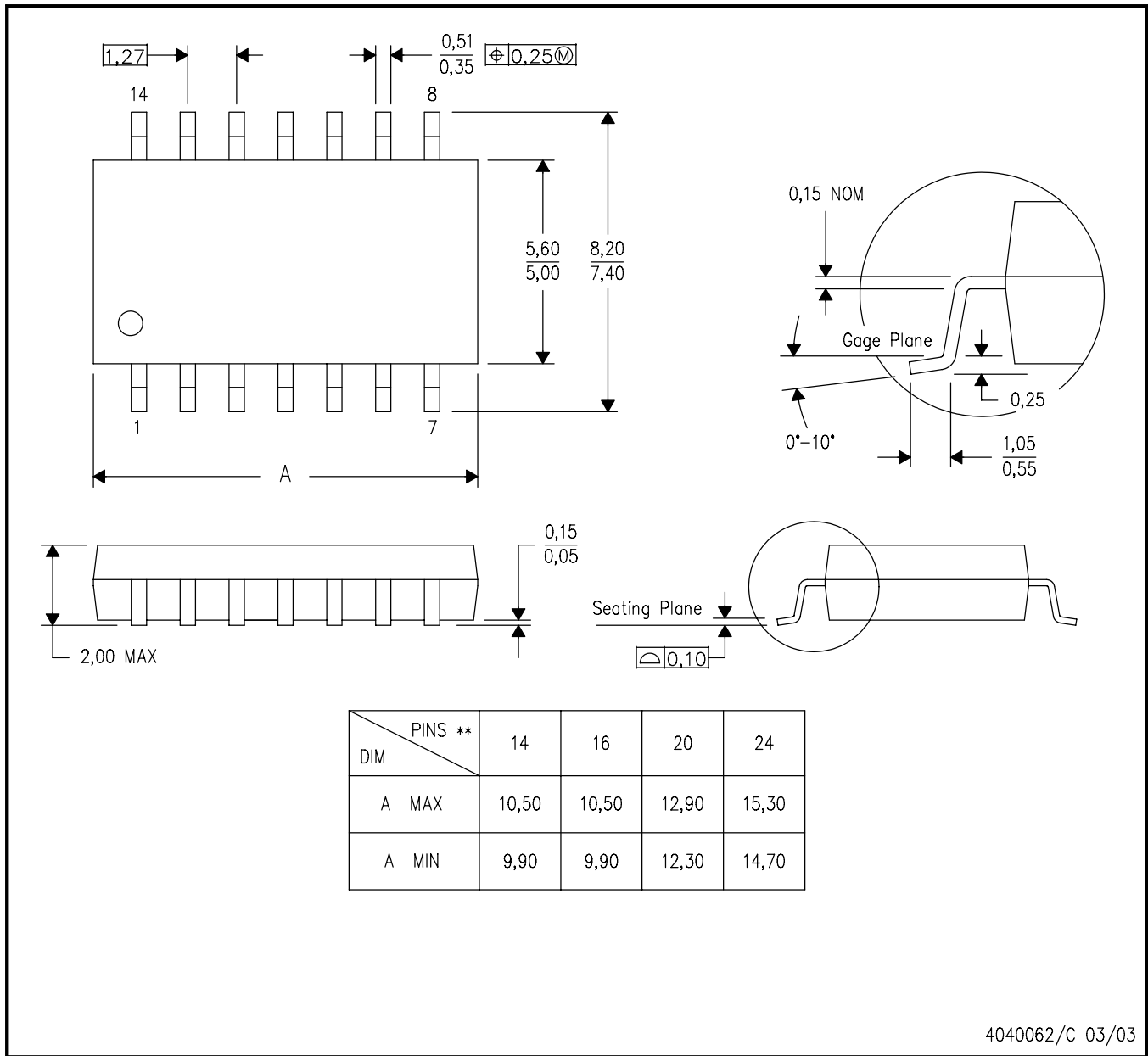
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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