SNx4HC245 具有三态输出的八路总线收发器

1 特性

- 2V 至 6V 的宽工作电压范围
- 高电流三态输出直接驱动总线或多达 15 个 LSTTL 负载
- 低功耗，最大 I_{CC} 为 80 µ A
- t_{pd} 典型值 = 12 ns
- ±6mA 输出驱动（电压为 5V 时）
- 低输入电流最大值为 1µA
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数进行的测试。

2 应用

- 服务器
- PC 和笔记本电脑
- 网络交换机
- 可穿戴保健和健身设备
- 电信基础设施
- 电子销售终端

3 说明

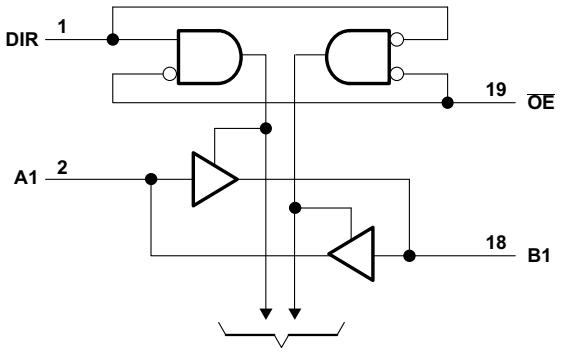
这些八路总线收发器专为数据总线之间的异步双向通信而设计。控制功能实现可更大限度地减少外部时序要求。

根据方向控制 (DIR) 输入上的逻辑电平，此类器件将数据从 A 总线发送至 B 总线，或者将数据从 B 总线发送至 A 总线。输出使能 ($\overline{OE}$) 输入可用于禁用器件，这样可有效隔离总线。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SNx4HC245	DB (SSOP, 20)	7.20mm × 5.30mm
	DW（SOIC、20）	12.80mm × 7.50mm
	N（PDIP、20）	24.33mm × 6.35mm
	NS (SO, 20)	12.60mm × 5.30mm
	PW（TSSOP，20）	6.50mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

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4 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (September 2015) to Revision F (August 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准	1

Changes from Revision D (August 2003) to Revision E (July 2015)	Page
• 添加了*器件比较* 部分、*热性能信息* 部分、*ESD 等级* 部分、*应用与实现*部分、*电源建议* 部分和*布局* 部分。	1
• 向“特性”列表中添加了“军用免责声明”。	1
• 更新了 FK 封装引脚排列图	3

5 引脚配置和功能

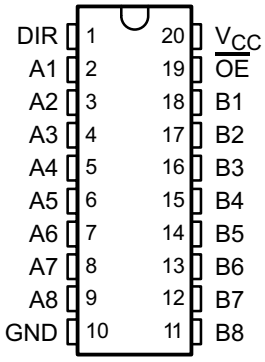


图 5-1. DB、DGV、DW、N、J、W 或 PW 封装 20 引脚 SSOP、TVSOP、SOIC、PDIP、CDIP、CFP 或 TSSOP 顶视图

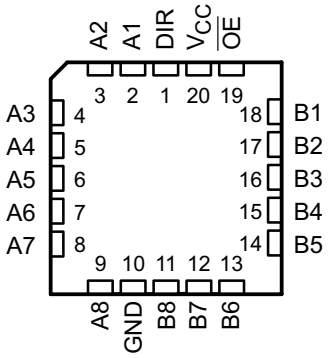


图 5-2. FK 封装 20 引脚 LCCC 顶视图

引脚		类型(1)	说明
编号	名称		
1	DIR	I/O	方向引脚
2	A1	I/O	A1 输入/输出
3	A2	I/O	A2 输入/输出
4	A3	I/O	A3 输入/输出
5	A4	I/O	A4 输入/输出
6	A5	I/O	A5 输入/输出
7	A6	I/O	A6 输入/输出
8	A7	I/O	A7 输入/输出
9	A8	I/O	A8 输入/输出
10	GND	—	接地引脚
11	B8	I/O	B8 输入/输出
12	B7	I/O	B7 输入/输出
13	B6	I/O	B6 输入/输出
14	B5	I/O	B5 输入/输出
15	B4	I/O	B4 输入/输出
16	B3	I/O	B3 输入/输出
17	B2	I/O	B2 输入/输出
18	B1	I/O	B1 输入/输出
19	OE	I/O	输出使能
20	VCC	—	电源引脚

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出

6 规格

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压		−0.5	7	V
I_{IK}	输入钳位电流(2)	$V_I < 0$ 或 $V_I > V_{CC}$		±20	mA
I_{OK}	输出钳位电流(2)	$V_O < 0$ 或 $V_O > V_{CC}$		±20	mA
I_O	持续输出电流	$V_O = 0$ 至 V_{CC}		±35	mA
	通过 V_{CC} 或 GND 的持续电流			±70	mA
T_{stg}	存储温度		−65	150	°C
T_J	结温			150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成损坏。这些仅为压力额定值，并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

6.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型（HBM），符合 ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议的操作条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN54HC245			SN74HC245			单位
			最小值	标称值	最大值	最小值	标称值	最大值	
V_{CC}	电源电压		2	5	6	2	5	6	V
V_{IH}	高电平输入电压	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	低电平输入电压	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	输入电压		0		V_{CC}	0		V_{CC}	V
V_O	输出电压		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	输入转换上升和下降时间	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5V			500			500	
		V_{CC} = 6 V			400			400	
T_A	自然通风条件下的工作温度范围		-55		125	−40		85	°C

(1) 器件所有的未使用输入必须被保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告*慢速或浮点 CMOS 输入的影响*，文献编号 SCBA004。

6.4 热性能信息

热指标(1)		SNx4HC245					单位
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 引脚					
$R_{\theta JA}$	结至环境热阻	92.1	77.0	57.0	74.1	99.7	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	53.9	41.5	48.6	40.6	34.0	°C/W
$R_{\theta JB}$	结至电路板热阻	47.2	44.8	38.0	41.6	50.7	°C/W
ψ_{JT}	结至顶部特征参数	16.5	16.8	25.4	14.8	1.8	°C/W
ψ_{JB}	结至电路板特征参数	46.8	44.3	37.8	41.2	50.1	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告，SPRA953。

6.5 电气特性

在推荐的自然通风条件下的工作温度范围（除非另外注明）

参数			测试条件		V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		单位
						最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	高电平输出电压		V_I = V_{IH} 或 V_{IL}	I_{OH} = –20μA	2V	1.9	1.998		1.9		1.9		V
					4.5V	4.4	4.499		4.4		4.4		
					6V	5.9	5.999		5.9		5.9		
				I_{OH}=-6 mA	4.5V	3.98	4.3		3.7		3.84		
				I_{OH}=-7.8 mA	6V	5.48	5.8		5.2		5.34		
V_{OL}	低电平输出电压		V_I = V_{IH} 或 V_{IL}	I_{OL} = 20μA	2V		0.002	0.1		0.1		0.1	V
					4.5V		0.001	0.1		0.1		0.1	
					6V		0.001	0.1		0.1		0.1	
				I_{OL} = 6 mA	4.5V		0.17	0.26		0.4		0.33	
				I_{OL} = 7.8 mA	6V		0.15	0.26		0.4		0.33	
I_I	输入电流	DIR 或 $\overline{OE}$	V_I = V_{CC} 或 0		6V		±0.1	±100		±1000		±1000	nA
I_{OZ}	关闭状态（高阻抗状态）输出电流	A 或 B	V_O = V_{CC} 或 0		6V		±0.01	±0.5		±10		±5	μA
I_{CC}	电源电流		V_I = V_{CC} 或 0，	I_O = 0	6V			8		160		80	μA
C_i	输入电容	DIR 或 $\overline{OE}$			2V 至 6V		3	10		10		10	pF

6.6 开关特性，C_L = 50pF

在建议的自然通风条件下的工作温度范围内（除非另有说明）
（请见图 7-1）

参数	从（输入）	至（输出）	V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A 或 B	B 或 A	2V		40	105		160		130	ns
			4.5V		15	21		32		26	
			6V		12	18		27		22	
t_{en}	$\overline{OE}$	A 或 B	2V		125	230		340		290	ns
			4.5V		23	46		68		58	
			6V		20	39		58		49	
t_{dis}	$\overline{OE}$	A 或 B	2V		74	200		300		250	ns
			4.5V		25	40		60		50	
			6V		21	34		51		43	
t_t		A 或 B	2V		20	60		90		75	ns
			4.5V		8	12		18		15	
			6V		6	10		15		13	

6.7 开关特性，C_L = 150pF

在建议的自然通风条件下的工作温度范围内（除非另有说明）
（请见图 7-1）

参数	从（输入）	至（输出）	V_{CC}	T_A = 25°C			SN54HC245		SN74HC245		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A 或 B	B 或 A	2V		54	135		200		170	ns
			4.5V		18	27		40		34	
			6V		15	23		34		29	
t_{en}	$\overline{OE}$	A 或 B	2V		150	270		405		335	ns
			4.5V		31	54		81		67	
			6V		25	46		69		56	
t_t		A 或 B	2V		45	210		315		265	ns
			4.5V		17	42		63		53	
			6V		13	36		53		45	

6.8 工作特性

T_A = 25°C

参数		测试条件	典型值	单位
C_{pd}	每个收发器的功率耗散电容	无负载	40	pF

6.9 典型特性

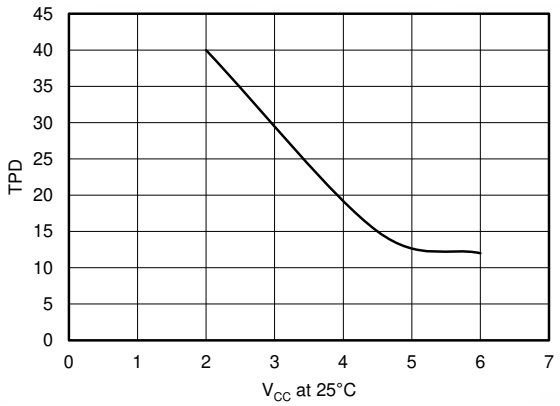


图 6-1. 25°C 时 TPD 与 V_{CC} 间的关系

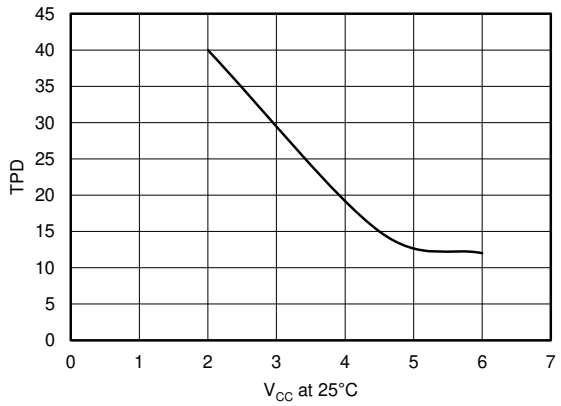
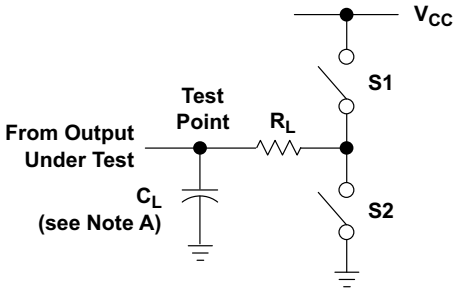


图 6-2. 25°C 时 TPD 与 V_{CC} 间的关系

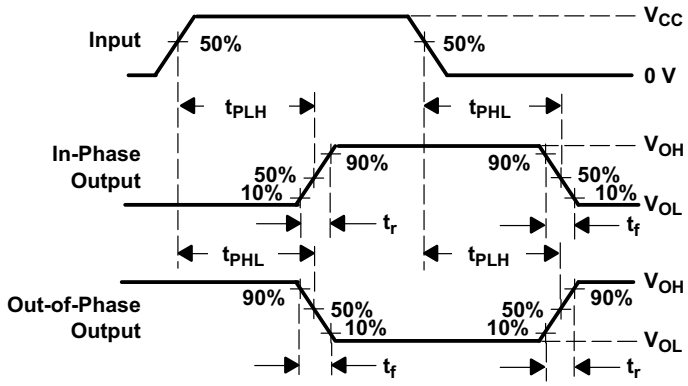
7 参数测量信息

7.1

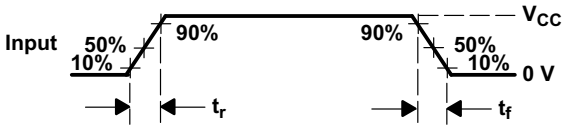


LOAD CIRCUIT

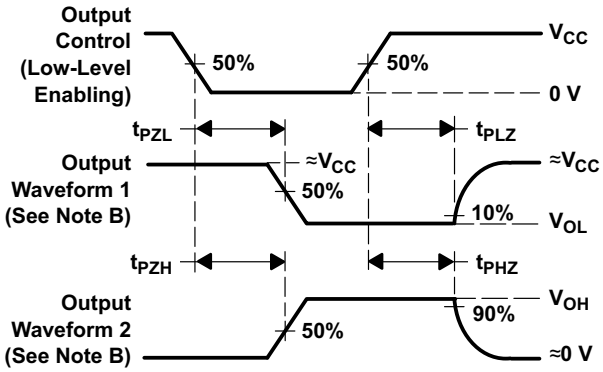
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. C_L 包括探头和测试夹具电容。
B. 波形 1 用于具有内部条件的输出，使得输出为低电平，除非被输出控制禁用。
波形 2 用于具有内部条件的输出，使得输出为高电平，除非被输出控制禁用。
C. 任意选择波形之间的相位关系。所有输入脉冲由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50 Ω，t_r = 6ns，t_f = 6ns。
D. 一次测量一个输出，每次测量一个输入转换。
E. t_{PLZ} 和 t_{PHZ} 与 t_{dis} 一样。
F. t_{PZL} 和 t_{PZH} 与 t_{en} 一样。
G. t_{PLH} 和 t_{PHL} 与 t_{pd} 一样。

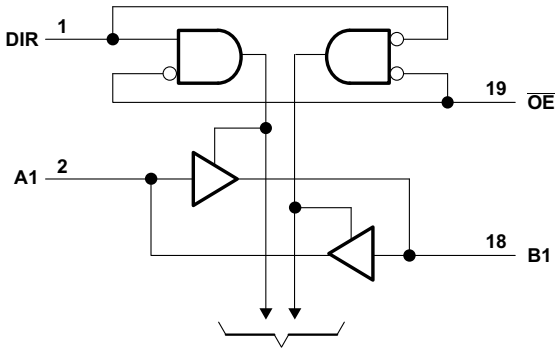
图 7-1. 负载电路和电压波形

8 详细说明

8.1 概述

这些八路总线收发器专为数据总线之间的异步双向通信而设计。控制功能实现可更大限度地减少外部时序要求。根据方向控制 (DIR) 输入上的逻辑电平，SNx4HC245 器件将数据从 A 总线发送至 B 总线，或者将数据从 B 总线发送至 A 总线。输出使能 (OE) 输入可用于禁用器件，这样可有效隔离总线。为确保在上电或掉电期间均处于高阻抗状态，应将 OE 通过上拉电阻器连接到 VCC；该电阻器的最小值取决于驱动器的灌电流能力。

8.2 功能框图



逻辑图（正逻辑）

8.3 特性说明

SNx4HC245 器件具有从 2V 到 6V 的宽工作 VCC 范围和较慢的边沿速率，以更大限度地减少输出振铃。

8.4 器件功能模式

表 8-1 列出了 SNx4HC245 的功能模式。

表 8-1. 功能表

输入 (1)		操作
$\overline{OE}$	DIR	
低电平	L	B 数据到 A 总线
低电平	高电平	A 数据到 B 总线
H	X	隔离

(1) H = 高电压电平，L = 低电压电平，X = 不用考虑

9 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 应用信息

SNx4HC245 是一款低驱动 CMOS 器件，可用于需要考虑输出振铃的多种总线接口类型应用。低驱动和慢速边沿速率将更大限度地减少输出上的过冲和下冲。

9.2 典型应用

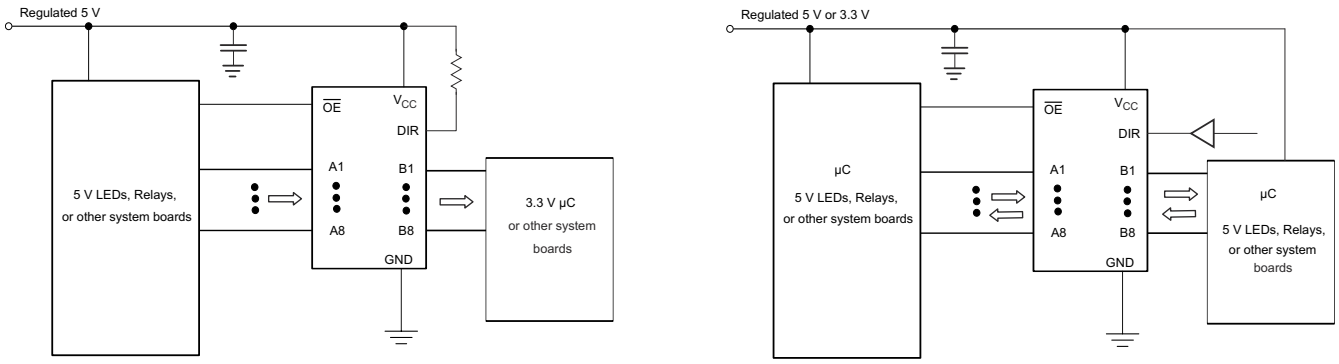


图 9-1. 典型应用原理图

9.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。可以组合输出以产生更高的驱动，但高驱动也会在轻负载时产生更快的边缘，因此应考虑路由和负载条件以防止振铃。

9.2.2 详细设计过程

1. 建议的输入条件
   - 上升时间和下降时间规格：请参阅 *节 6.3* 中的 ($\Delta t / \Delta V$)。
   - 指定了高电平和低电平：请参阅 *节 6.3* 中的 (V_{IH} 和 V_{IL}) 。
2. 建议的输出条件
   - 每个输出的负载电流不应超过 25mA，该器件的总电流不应超过 75mA。
   - 输出不应被拉至高于 V_{CC}。

9.2.3 应用曲线

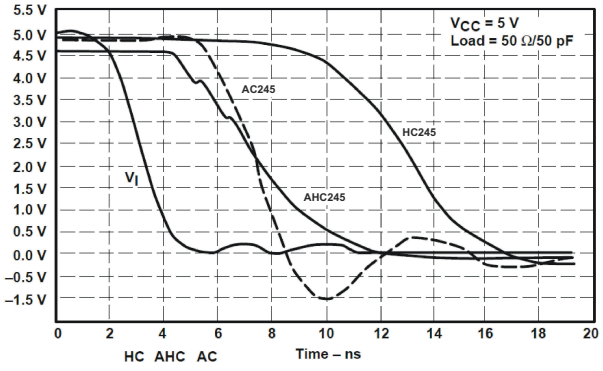


图 9-2. 开关特性比较

10 电源相关建议

电源可以是 *节 6.3* 中最小和最大电源电压额定值之间的任意电压。

每个 V_{CC} 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 μf；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 0.01 μf 或 0.022 μf。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 μf 和 1 μf 通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

11 布局

11.1 布局指南

当使用多位逻辑器件时，输入不应悬空。

在许多情况下，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时，未使用数字逻辑器件的功能或部分功能。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的操作状态。图 11-1 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须被连接至一个高或低偏置以防止它们悬空。应应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，它们将连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。浮动输出通常是可以接受的，除非该器件是收发器。如果收发器有一个输出使能引脚，它会在置位时禁用该器件的输出部分。这不会禁用 IO 的输入部分，因此它们在禁用后不能浮动。

11.2 布局示例

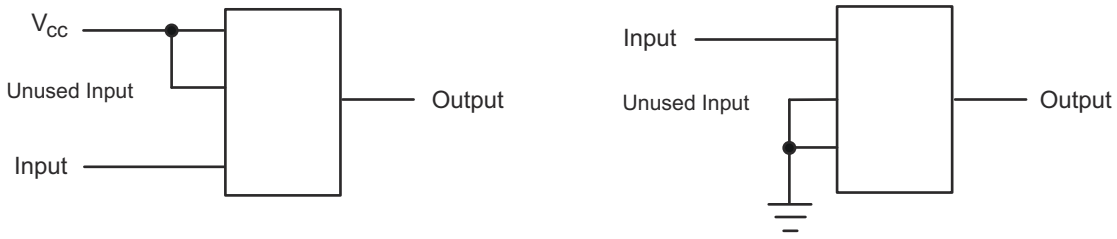


图 11-1. 布局图

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 12-1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
SN54HC245	点击此处	点击此处	点击此处	点击此处	点击此处
SN74HC245	点击此处	点击此处	点击此处	点击此处	点击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8408501VRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8408501VR A SNV54HC245J	Samples
5962-8408501VSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8408501VS A SNV54HC245W	Samples
84085012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84085012A SNJ54HC 245FK	Samples
8408501RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501RA SNJ54HC245J	Samples
8408501SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501SA SNJ54HC245W	Samples
JM38510/65503BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BRA	Samples
JM38510/65503BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BSA	Samples
M38510/65503BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BRA	Samples
M38510/65503BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BSA	Samples
SN54HC245J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC245J	Samples
SN74HC245DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245DBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC245N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC245N	Samples
SN74HC245NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245NSRE4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SN74HC245PWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	Samples
SNJ54HC245FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84085012A SNJ54HC 245FK	Samples
SNJ54HC245J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501RA SNJ54HC245J	Samples
SNJ54HC245W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501SA SNJ54HC245W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC245, SN54HC245-SP, SN74HC245 :

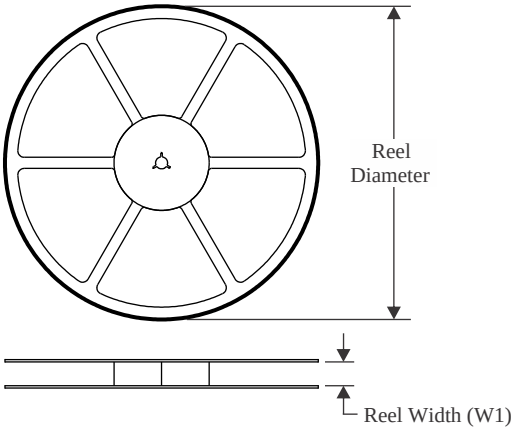
- Catalog : SN74HC245, SN54HC245
- Military : SN54HC245
- Space : SN54HC245-SP

NOTE: Qualified Version Definitions:

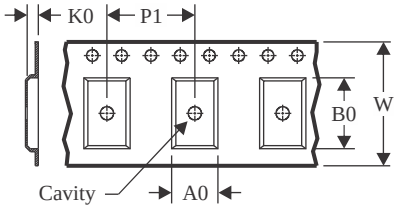
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

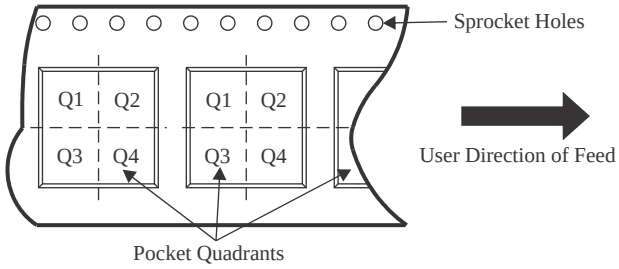


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

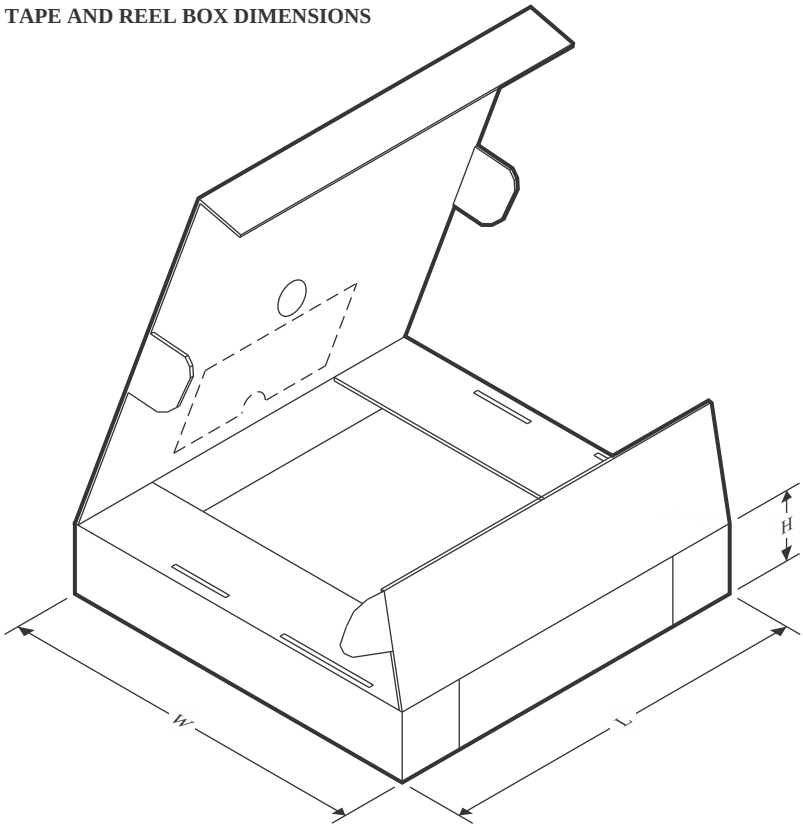
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HC245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC245PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

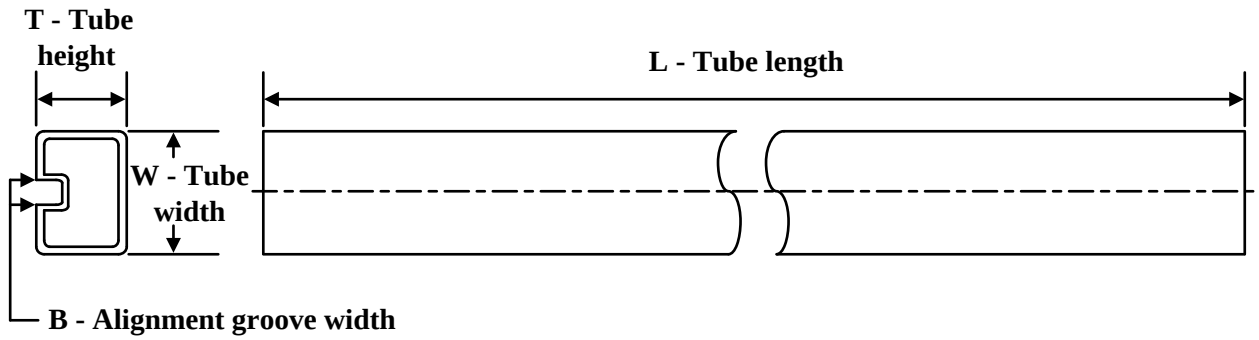
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC245DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC245NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC245PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74HC245PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC245PWT	TSSOP	PW	20	250	356.0	356.0	35.0

TUBE

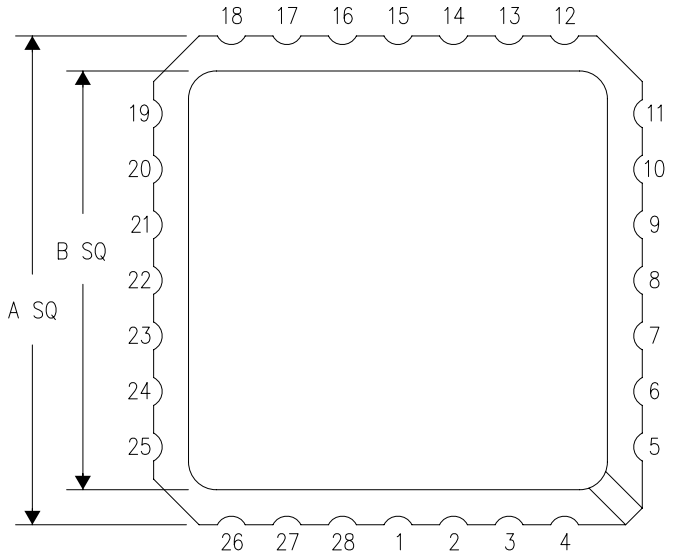


*All dimensions are nominal

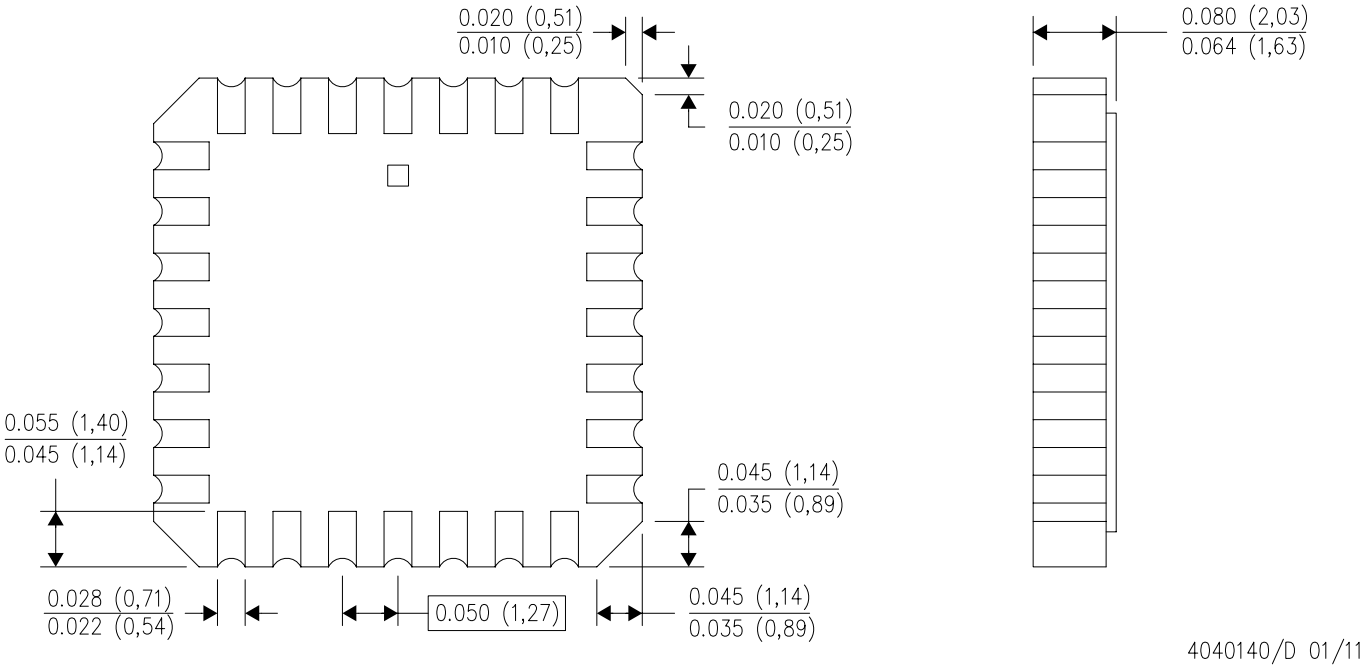
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8408501VSA	W	CFP	20	1	506.98	26.16	6220	NA
84085012A	FK	LCCC	20	1	506.98	12.06	2030	NA
8408501SA	W	CFP	20	1	506.98	26.16	6220	NA
JM38510/65503BSA	W	CFP	20	1	506.98	26.16	6220	NA
M38510/65503BSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74HC245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC245N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC245PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74HC245PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54HC245FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54HC245W	W	CFP	20	1	506.98	26.16	6220	NA

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

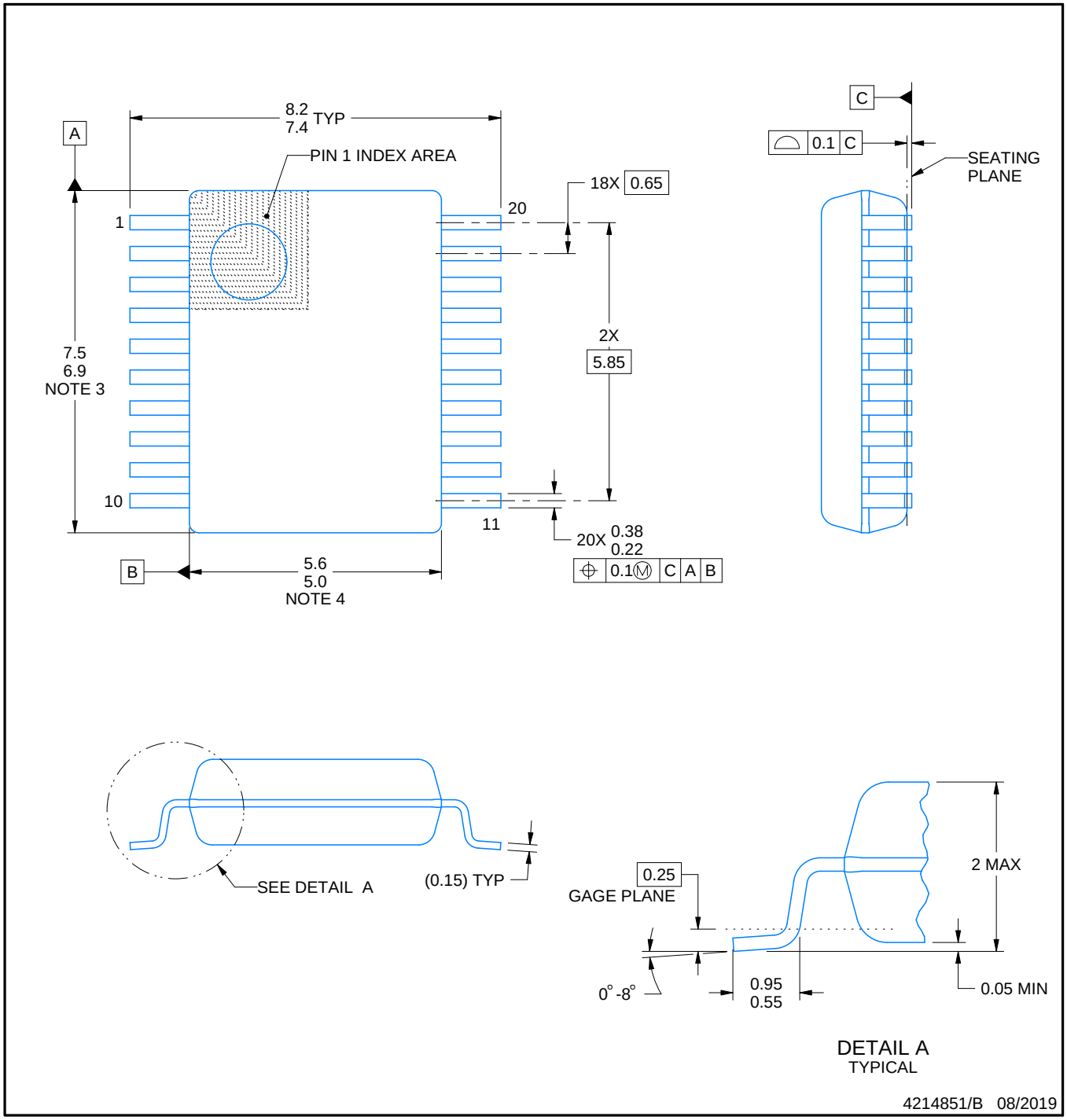
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

PACKAGE OUTLINE

DB0020A

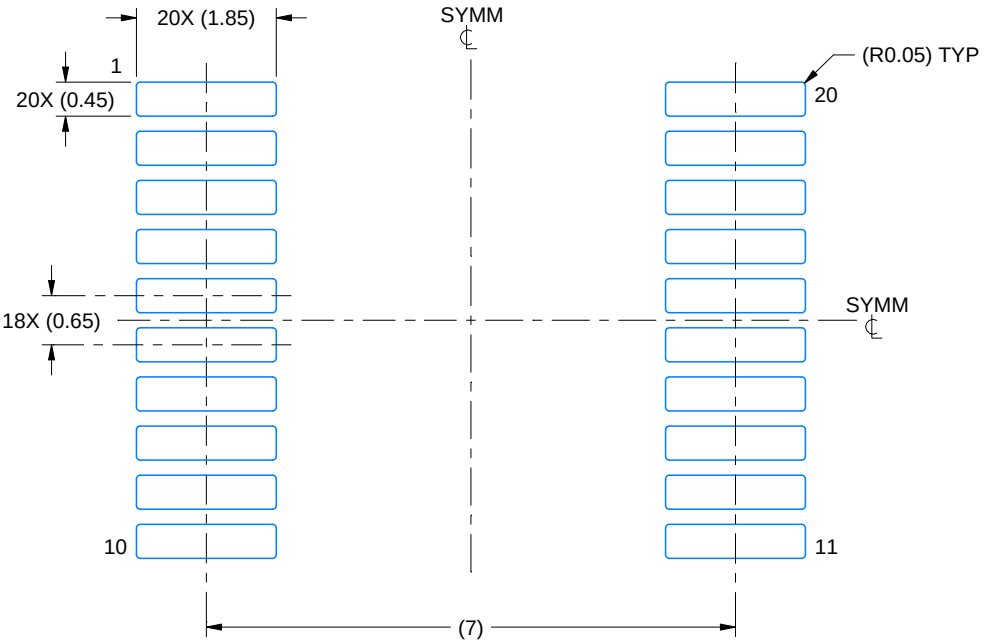
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

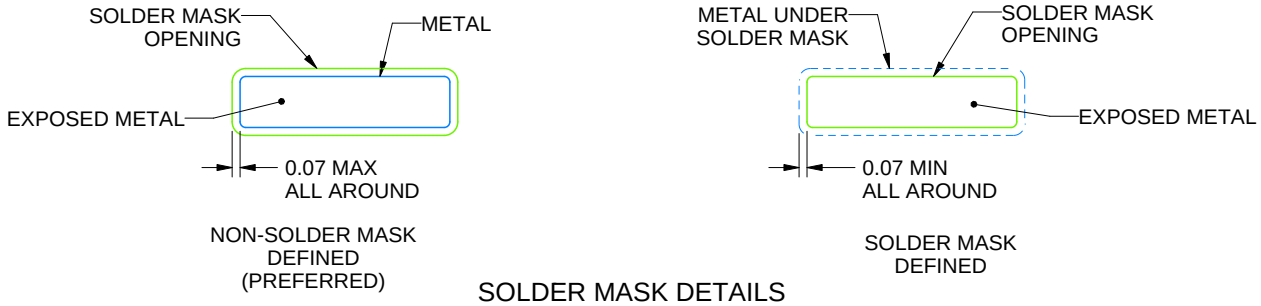


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

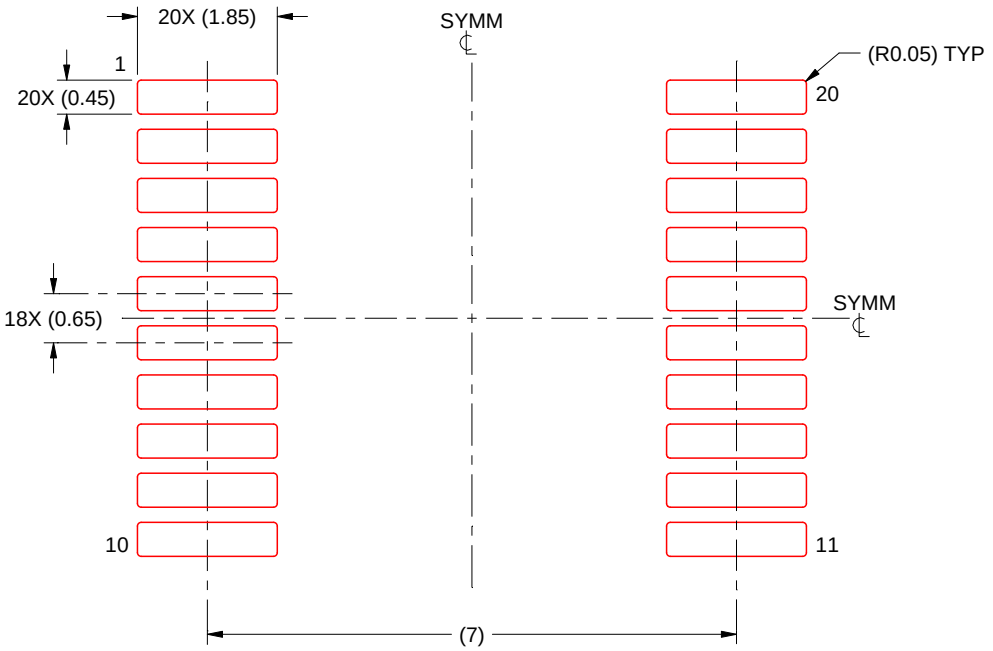
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

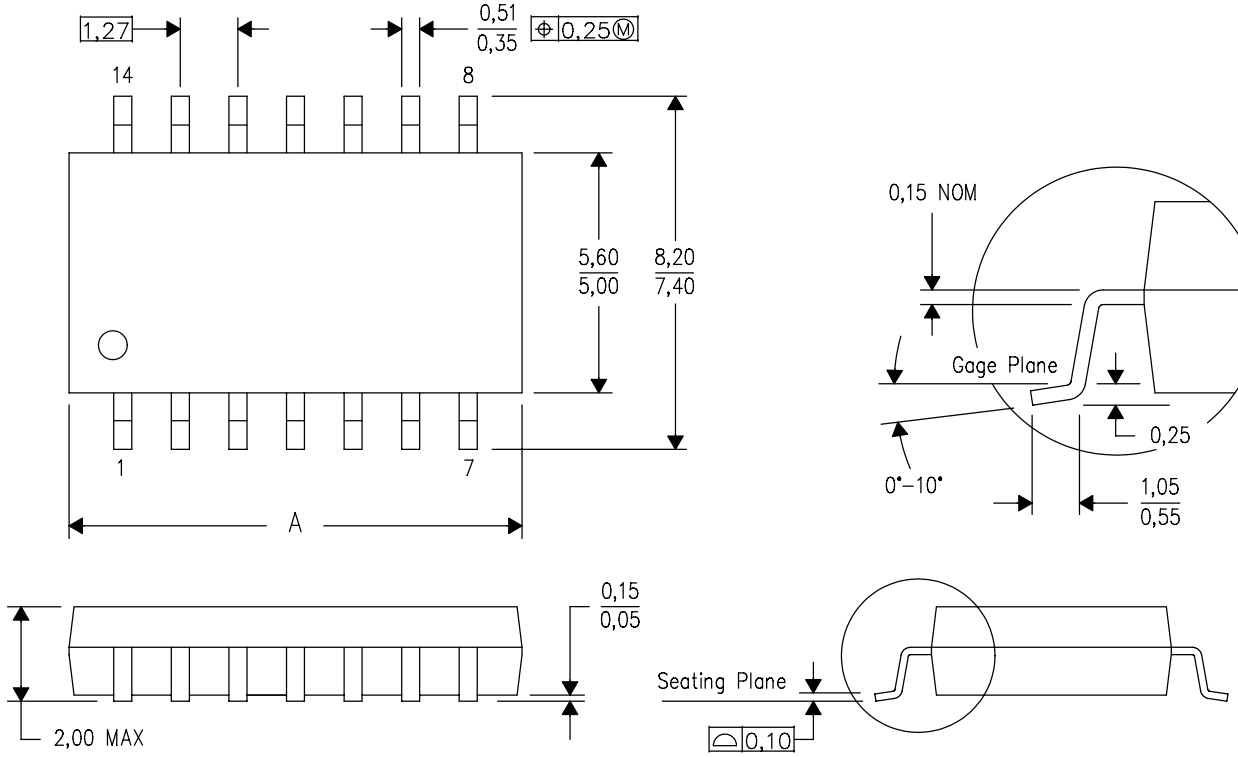
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

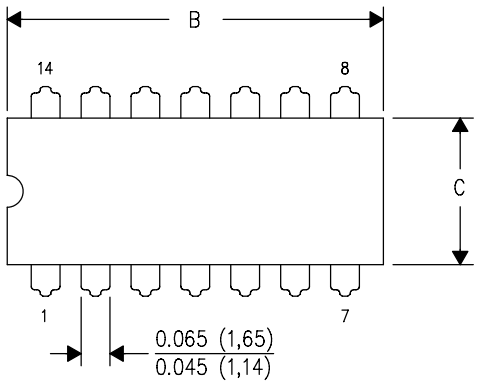
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

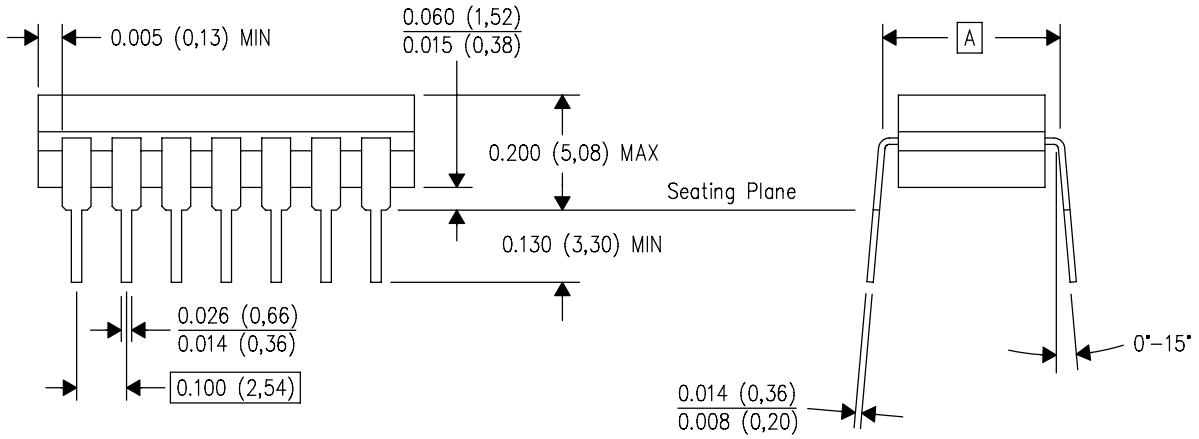
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



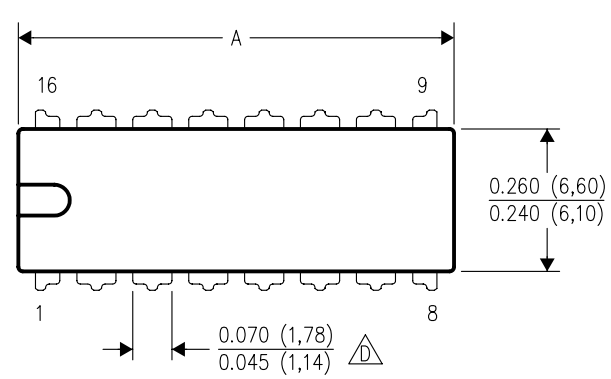
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

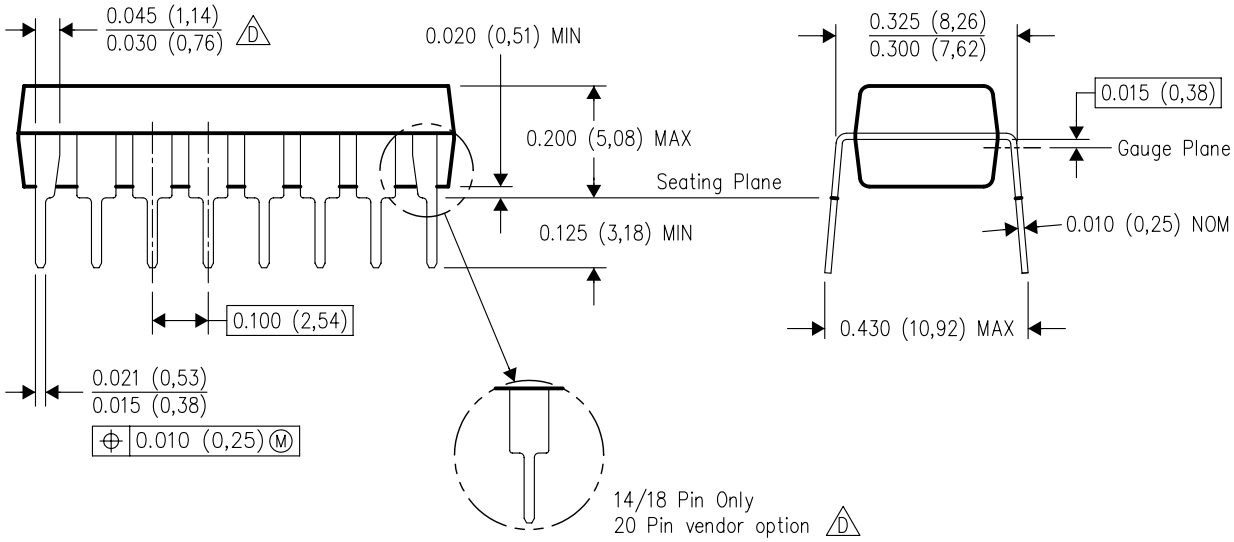
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

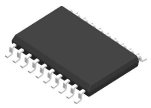


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

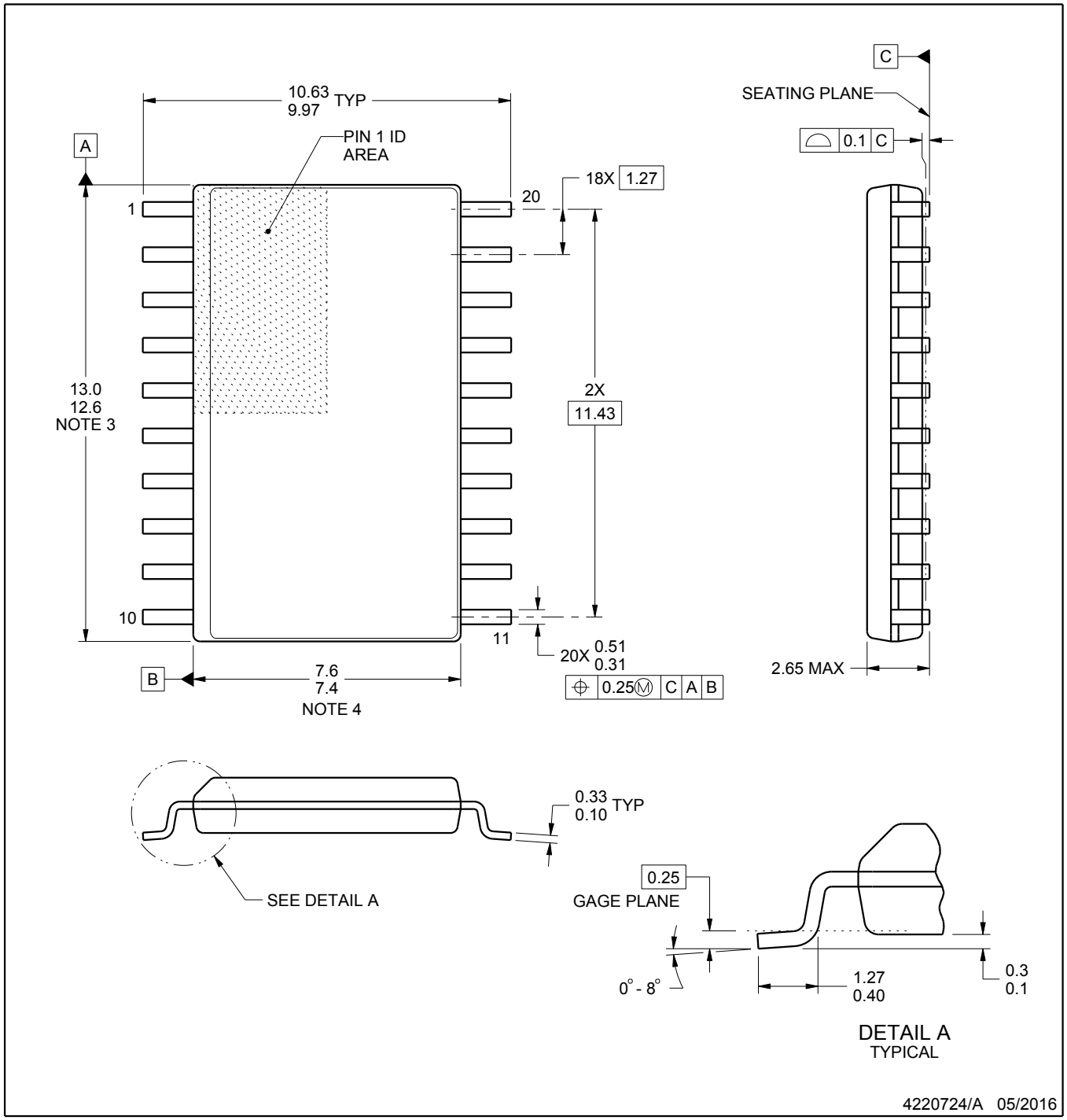


PACKAGE OUTLINE

DW0020A

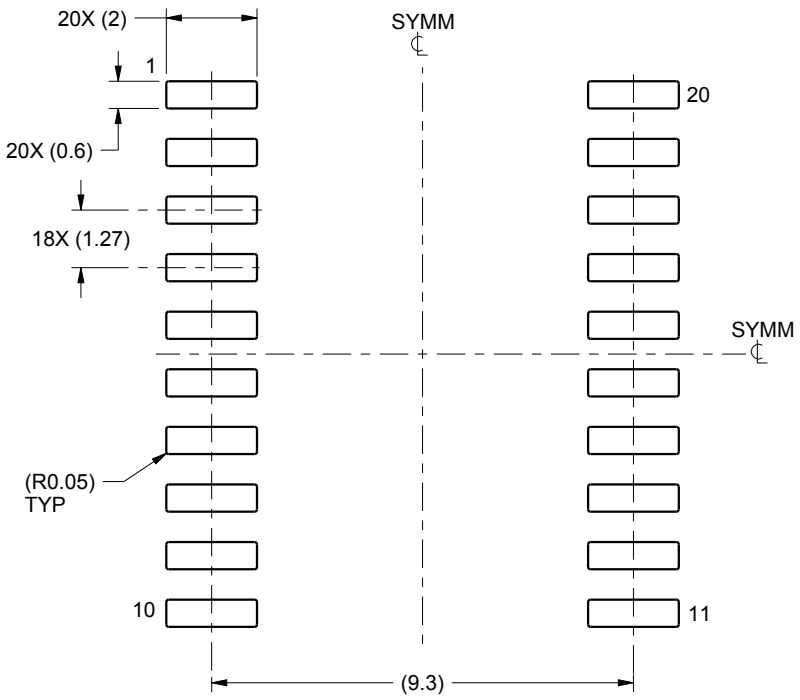
SOIC - 2.65 mm max height

SOIC

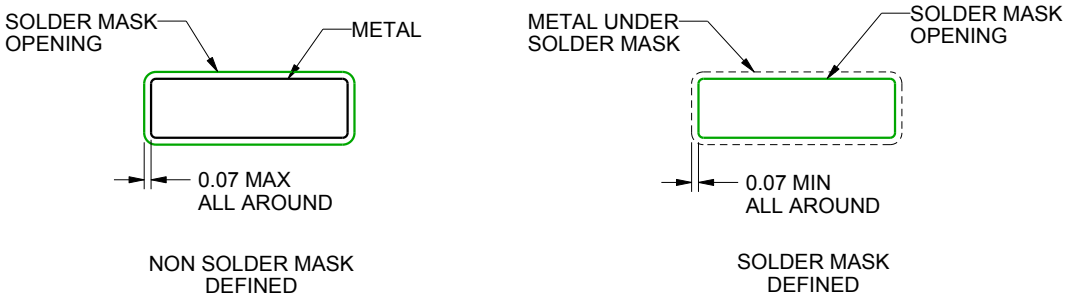


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

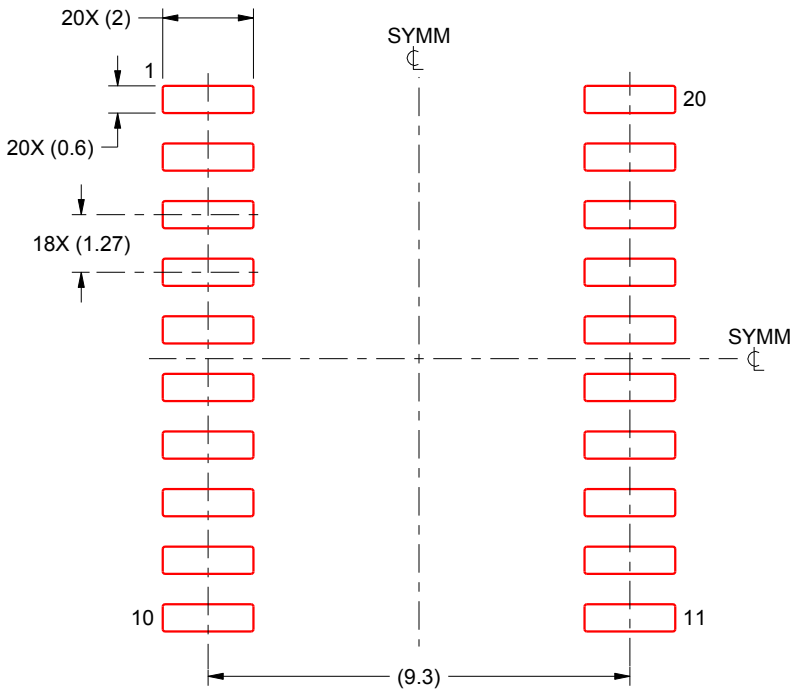


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



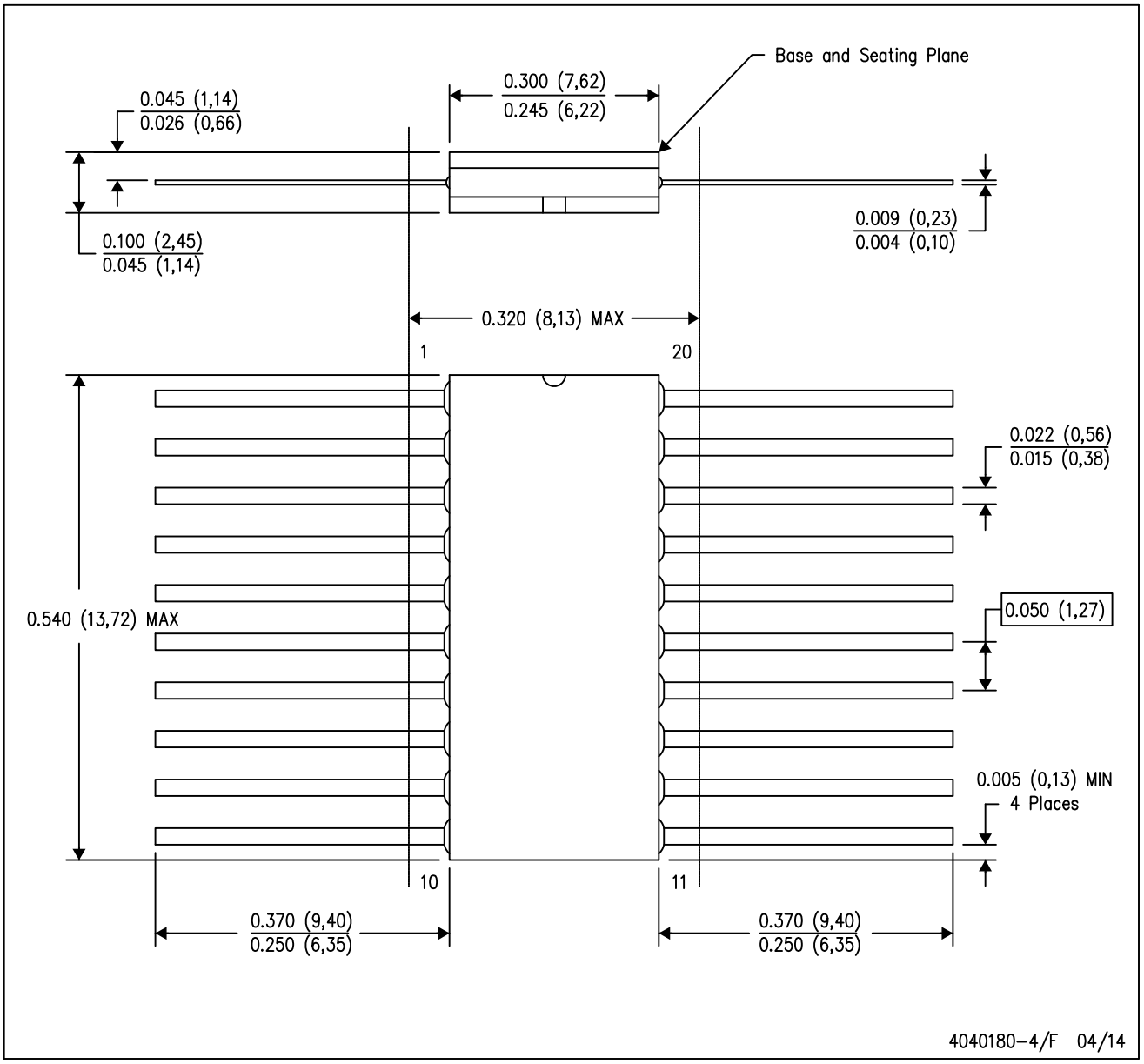
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



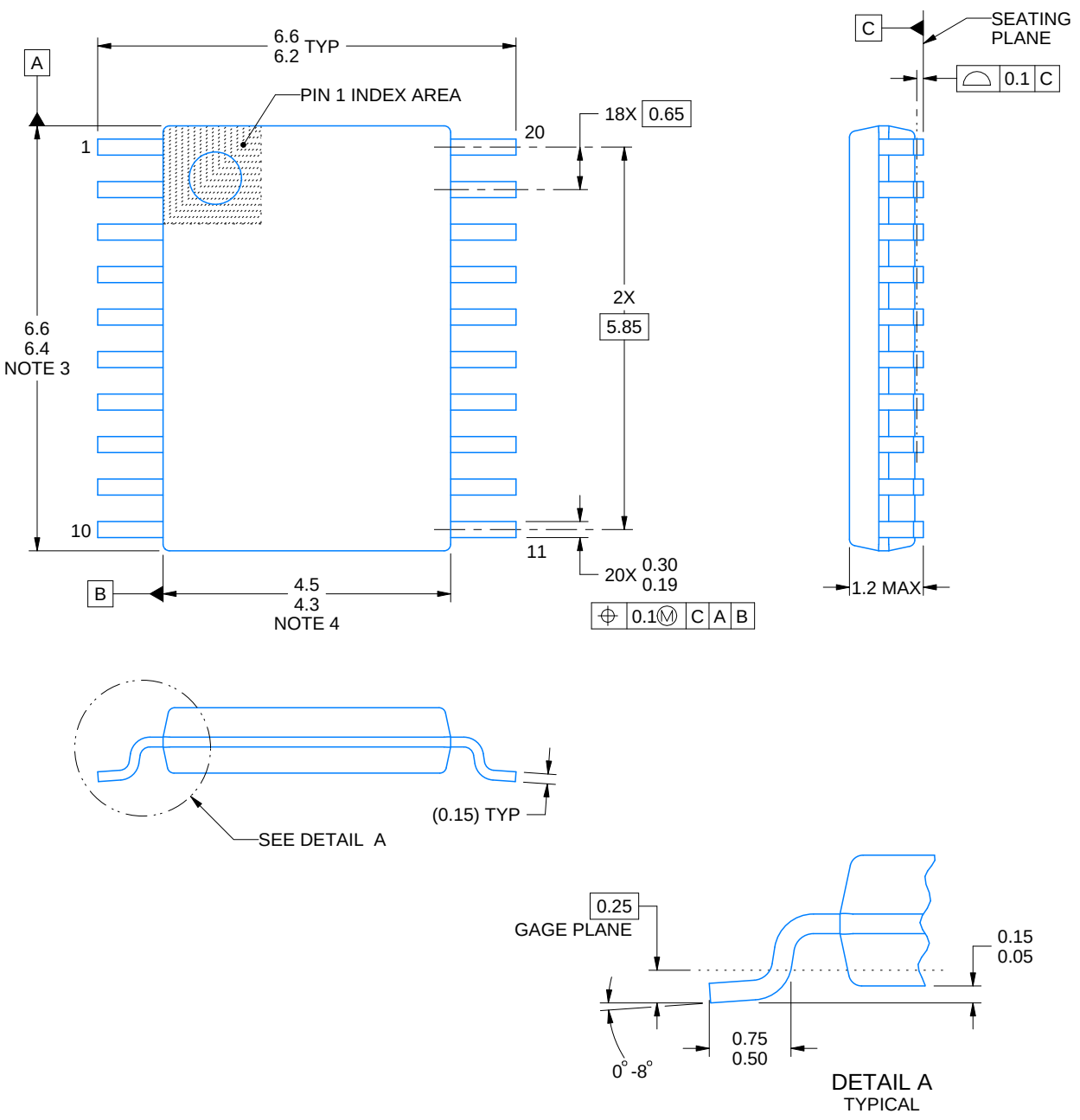
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

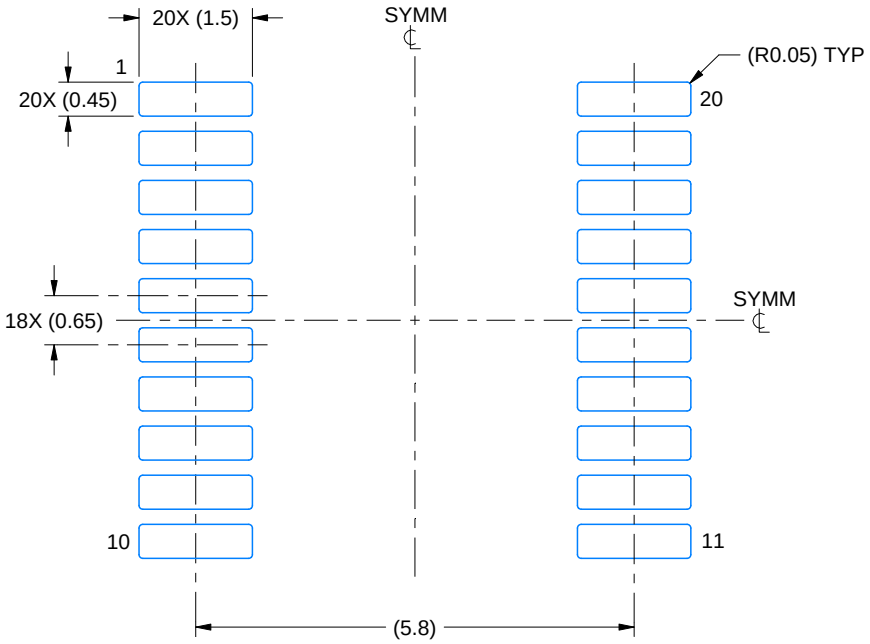
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



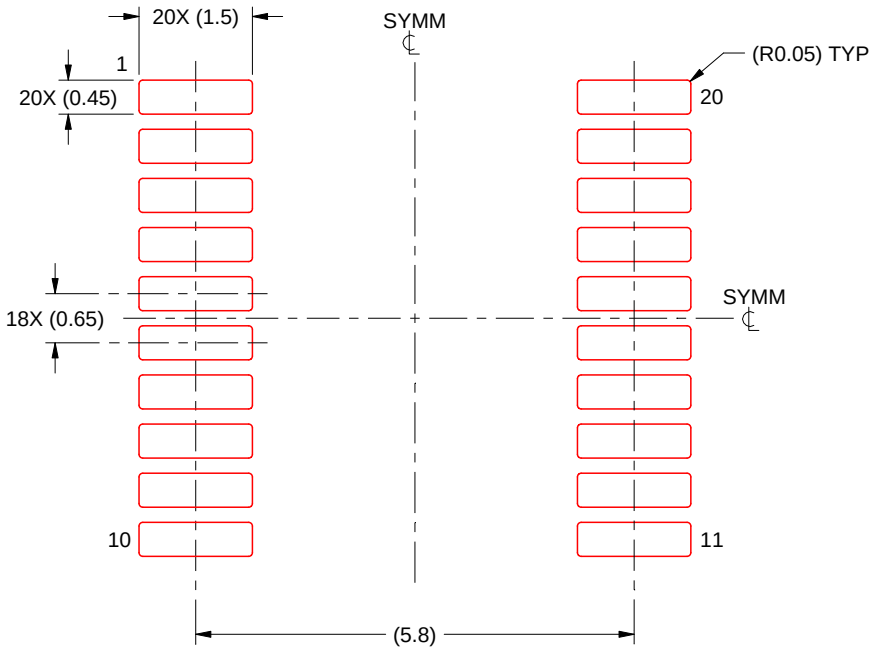
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



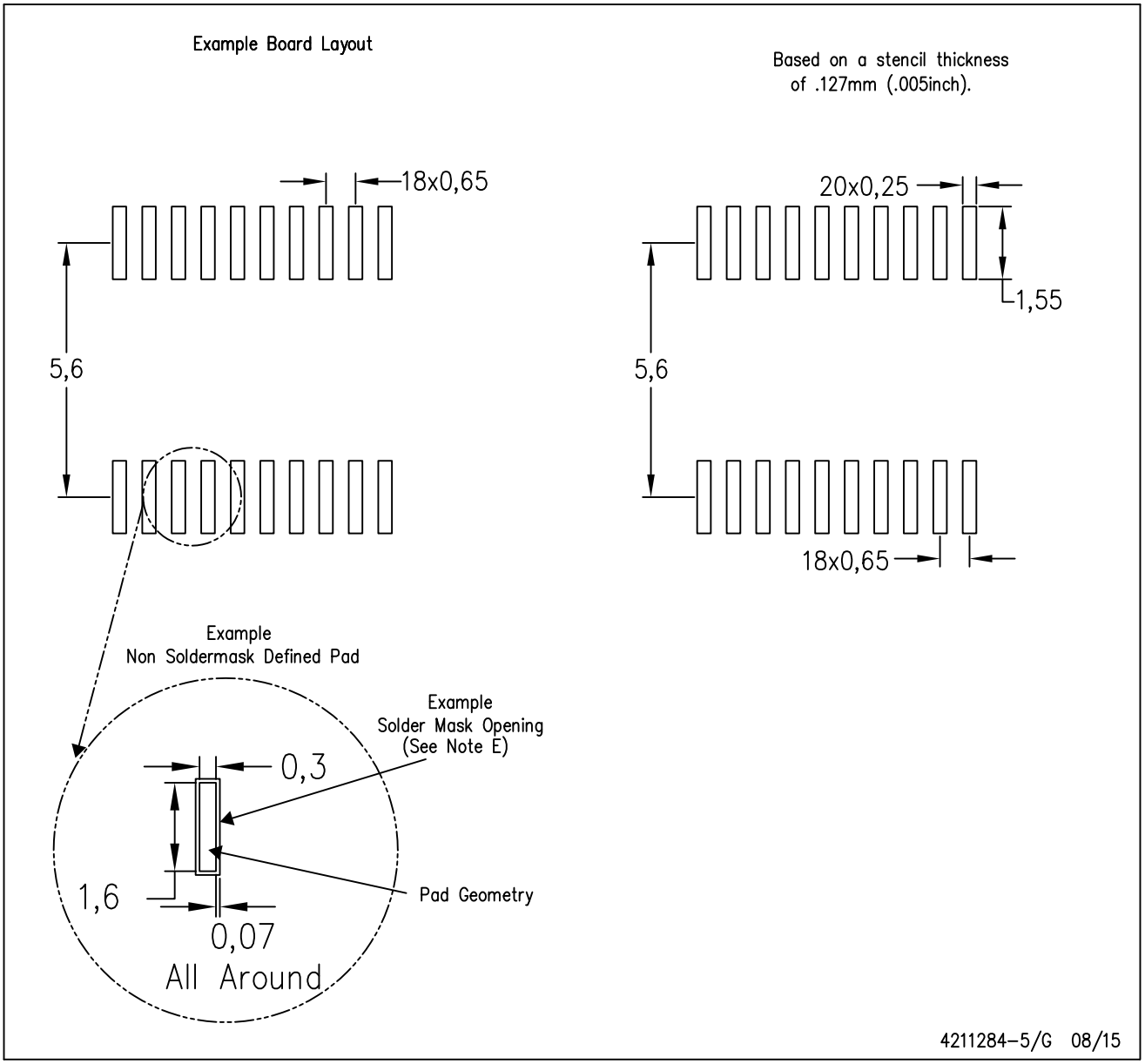
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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